Final Term Examination- Fall 2024

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Course :- CSE - 413

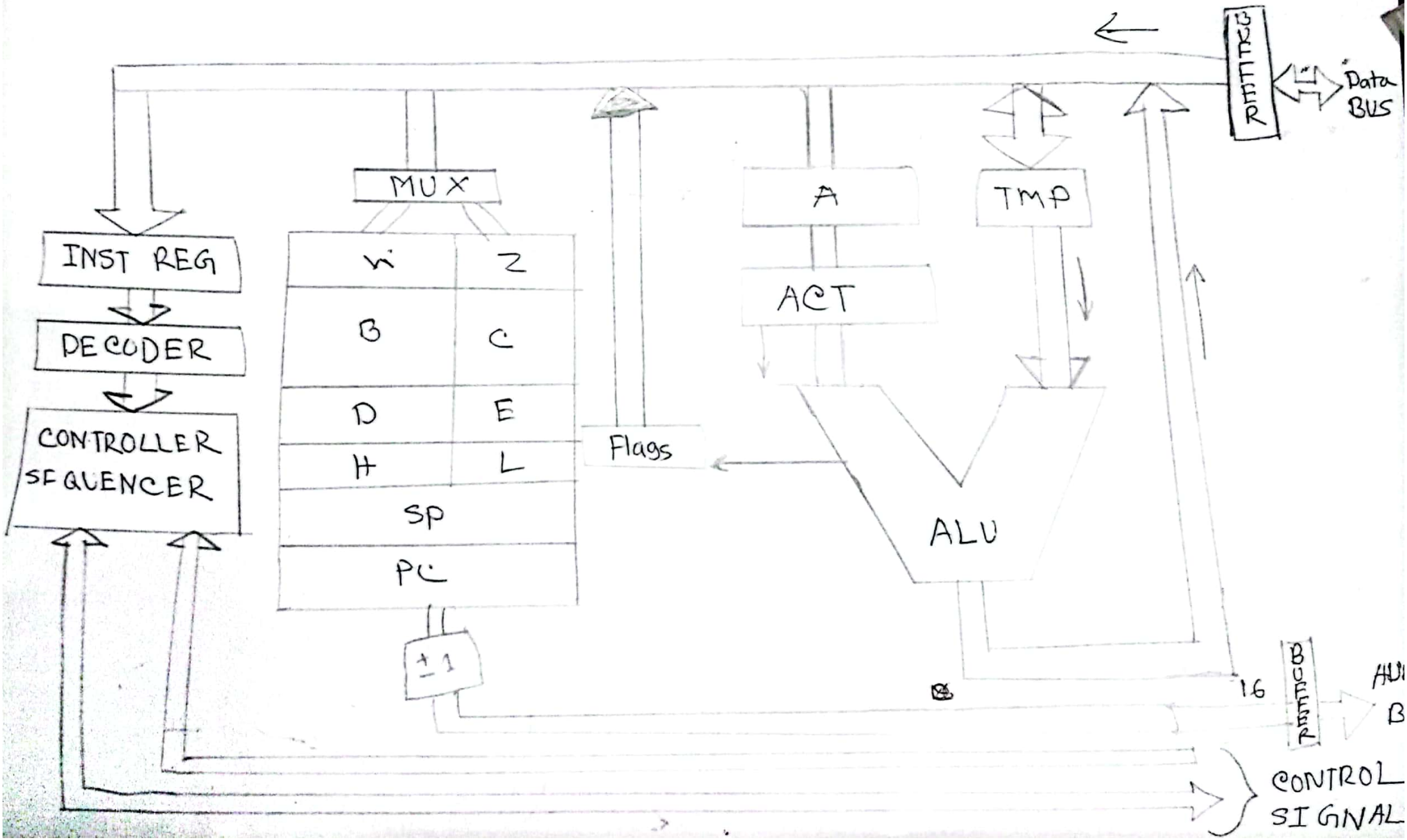
Subject :- Microprocessor

Dept :- CSE

1. NO. Que. Ans :-

a) ans :- **Address Bus :-** An address bus is a unidirectional set of wires that carry memory addresses from the CPU to memory or I/O devices, determining the location to read or write data.

Q.6 Ans:- The Microprocessor Architecture :-



1.c) ans :- List of steps in the Execute Cycle :-

The Execute Cycle is the phase of instruction execution in a microprocessor where the fetched and decoded instruction is executed. The specific steps depends on the instruction type (arithmetic, logical, memory, control etc but the general execution cycle includes :-

1. Opcode Execution :- The Control Unit activates the necessary circuits for the instruction.
2. Operand Fetch (if needed) - Date is retrieved from registers or memory.
3. ALU Operation - Arithmetic or logical computations are performed.
4. Memory Read/Write - Data is transferred betwee registers and memory.
5. Register Update - The result is stored in the appropriate registers.
6. Flags Update - The status flags (zero,

carry, overflow, etc), are modified if necessary.

7. Jump/ Branch – If the instruction involves branching the Program Counter (PC) is updated accordingly.

2. No. ans:

a) ans: BIU & EU

BIU

The Bus Interface Unit (BIU) handles data transfer between the processor and memory or I/O devices. It manages the address bus, data bus and control bus and perfoms instruction feteching, address calculation, and memory access.

EU

The Execution Unit (EU) is responsible for decoding and executing instructions. It includes the Arithmetic Logic Unit (ALU), registers and control circuitry to process data and perform computations.

Wait Mode :-

Wait Mode is a low-power state in which the processor halts execution while waiting an external event. The clock continues running, but the CPU stops executing instructions until it receives a wake-up signal. This helps in power saving while keeping peripherals active.

2.b) ans'l definition :-

The Intel 8086 microprocessor is a 16-bit processor with a segmented memory architecture. It consists of two main units.

1. Bus Interface Unit (BIU) - Handle memory and I/O operations.
2. Execution Unit (EU) - Executes instructions and processes data.

Key Capon Components :-

1. BIU - ⊛ Handle memory addressing

and fetching instructions.

*) Stores instructions in a 6-byte instruction queue for pipelining.

*) Manages segment registers (CS, DS, SS, ES) for memory segmentation.

2. Execution Unit (EU).

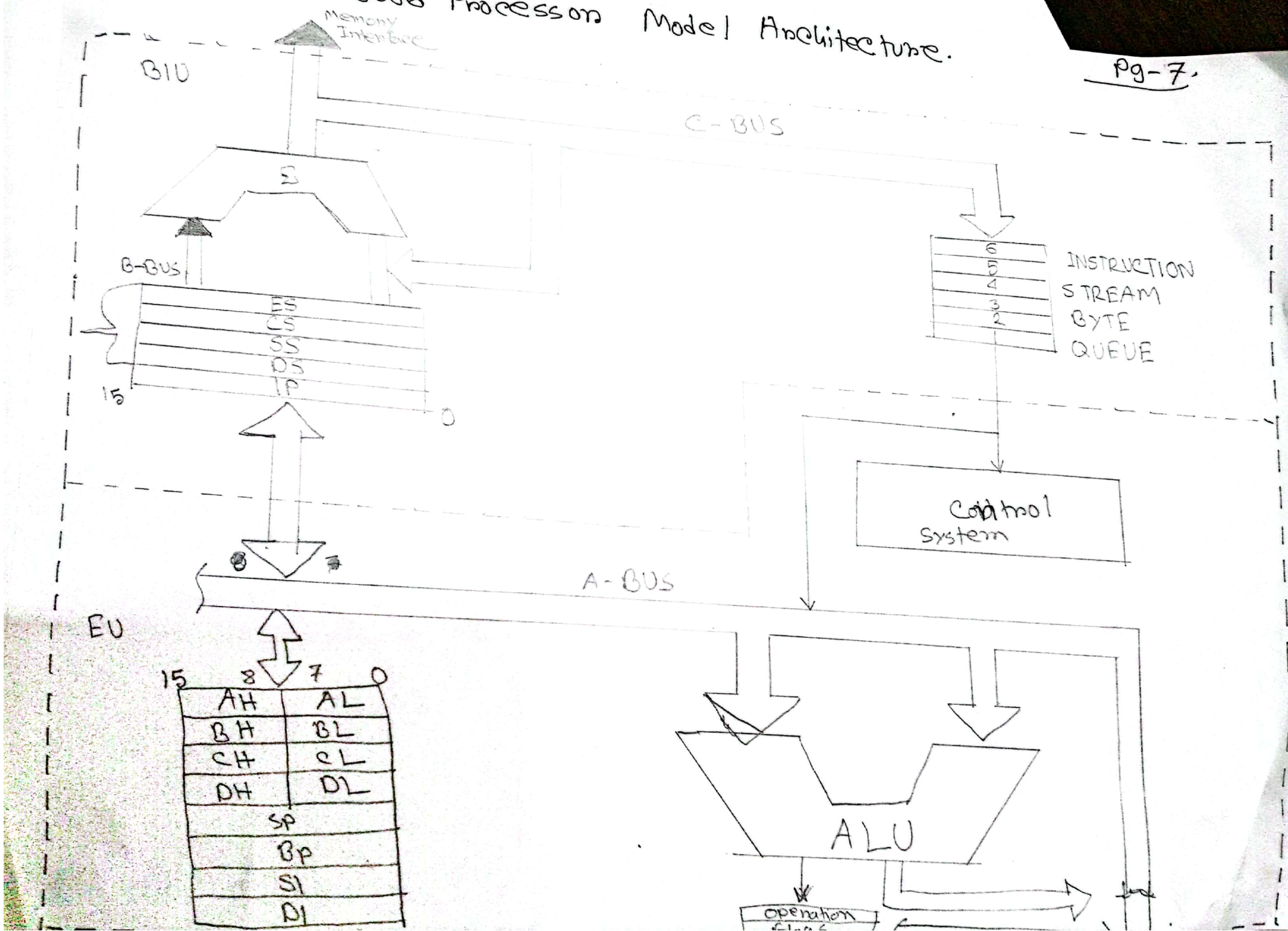
* Decodes and executes instruction.

* Contains the Arithmetic Logic Unit (ALU) for operations

* Uses general purpose registers (AX, BX, CX, DX) for computation.

* Updates flag registers (ZF, CF, SF, etc).

2.b) Ans: The 8086 Processor Model Architecture.



a) MOV AX, BX Instruction :-

The MOV AX, BX instruction in 8086 Assembly Language copies the 16-bit data from the BX register into the AX register.

* MOV - Transfer data instruction.
* AX → Destination register.
* BX → Source register.
* Effect : AX = BX (BX remains unchanged).

Example :- If BX = 1234 H, after execution, AX = 1234

b) ans:- Operation of MOV AL, [1234H] instruction.

The instruction loads the byte stored at memory address (DS:1234 H) into AL register.

1. Segment + offset Address calculation :-

* The physical memory address in 8086 is calculated as:

Physical Address = (DS x 16) + offset.

* Given DS = 1000H and offset = 1234 H, the physical address is:

$(1000H \times 16) + 1234H = 10000H + 1234H$

$= 11234H$

2. Memory Read Operation.

* The CPU reads the byte stored at memory address 11234H
* The content at address 11234H is moved into the AL register.

Memory Diagram Representation.

Memory Address	Stored Data
11234H	5AH (Example Data)

Before Execution:-

* AL = ?? (Unknown)

After Execution:-

* AL = 5AH (Content at 11234H is loaded into AL)

AL ← [11234H] : AL now holds the byte from memory.

c) ans:- Operation of the MOV AX, [BX] Instruction.

This instruction loads the word (16 bit) from memory at the address specified by the value in BX into the AX register.

step-by-step Execution:-

1. Segment:offset Address Calculation:-

* In 8086 the physical memory address is calculated as:

Physical Address = (segment Resisten x16)+ offset.

*) BX = 1000H (this is the offset), and DS=0100H (this is the segment).

* The physical address is.

(DSx16) + BX = (0100H x16) + 1000H = 1000H + 1000H = 2000H.

2. Memory Read Operation :-

* The CPU now heads the word stored at memory address 2000H and loads it into

the AX register.

Memory Diagram.

Memory Address	Stored Data
2000H	00H (Low byte)
2001H	01H (High byte).

Before Execution:-

* AX = ? (Unknown)

* After Execution

* AX = 0100H (The 16-bit value at memory location 2000H and 2001H is loaded into AX)

AX ← [2000H]; AX now holds the word from memory at address 2000H

Explanation of Data Transfer:

* The BX register holds the offset address 1000H.

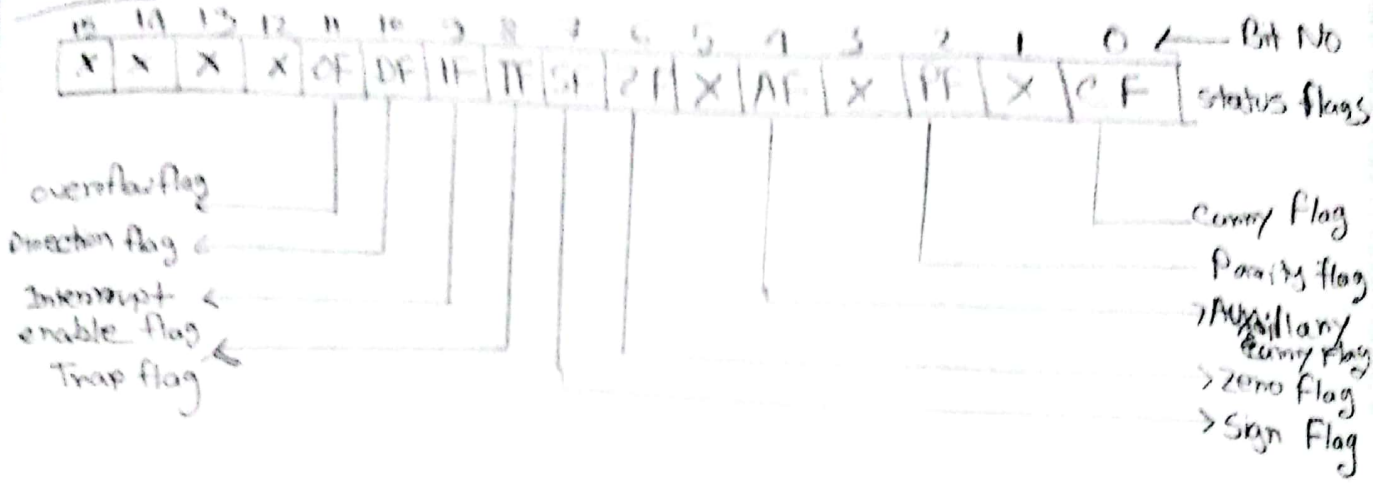
*) The DS register holds the segment 0100H.

*) The physical address is 2000H (DS x 16 + BX).

*) The data at memory address 2000H is read (00H in the low byte, 01H in the high byte), and then loaded into the AX register.

9.NO.Ques.Ans.1

Ans:



Description of Key Flags:

CF, The Carry Flag:- This Flag is set whenever there is a carry out, either from d7 after an 8-bit operation, or from d15 after a 16-bit data operation.

PF, the Parity Flag:- After certain operations, the parity of the result's low-order byte is checked. If the byte has an even number of 1s, the parity flag is set to 1; otherwise, it is cleared.

AF, the Auxillary Carry Flag:- If there is a carry from d3 to d4 of an operation this bit is set to 1, otherwise cleared (set to 0).

ZF, the Zero Flag :- The ZF is set to 1 if the result of the arithmetic or logical operation is zero, otherwise, it is cleared (set to 0).

SF, the Sign Flag :- MSB is used as the sign bit of the binary representation of the signed numbers. After arithmetic or logical operations the MSB is copied into SF to indicate the sign of the the result.

TF, the Trap Flag :- When this flag is set it allows the program to single step, meaning to execute one instruction at a time. Used for debugging purpose.

IF, Interrupt Enable Flag :- This bit is set or cleared to enable or disable only the external interrupt requests.

DF, the Direction Flag:- This bit is used to control the direction of the string operations.

OF, the Overflow Flag:- This flag is set whenever the result of a signed number operation is too large, causing the high-order bit to overflow into the sign bit.

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  34 F5          0011 0100 1111 0101
+ 95 EB        + 1001 0101 1110 1011
-------        ---------------------
  CA E0        1100 1010 1110 0000
```

4. b) ans: Status and Control Flags in 8086 Processor

1. Carry Flag (CF).

*) Bit: D0

* The Carry Flag is set when there is a carry out or borrow in arithmetic operations. It is used for operations that involve multiple-word or multi-byte arithmetic.

Usage: → * Set in addition when a carry is

generated beyond the

bit.

*) Set in subtraction when a borrow occurs.

Ex: In ADD AX, BX if the result exceeds the size of AX, CF will be set.

2. Zero Flag (ZF).

* Bit: 03

*) The Zero Flag is set if the result of an operation is zero. It indicates whether the result of an operation produces a zero value.

Usage:

* Used for comparison operations to check if two values are equal.

Ex: In SUB AX, AX, the result is zero, so ZF will be set.

3. Parity Flag (PF).

* Bit: D2

* The Parity Flag is set if the number

of 1 bits in the result of the last operation is even. If the number of 1s is odd, the flag is cleared.

* Usage:-

* Used for error detection in systems where even parity is required.

Ex: After an operation, if the binary result contains an even number of 1s, PF is set.

4. Sign Flag: (SF).

*) Bit: D4

* The Sign Flag is set if the most significant bit (MSB) of the result is 1, indicating a negative number in two's complement representation. It reflects the sign of the result.

* Usage:

* Often used for signed number operations to check if the result is positive or negative.

Ex; In ADD, AX, BX ; if the result is negative SF will be set

5. Interrupt Flag (IF).

* Bit : 06

*) The Interrupt Flag is used to enab or disable interrupts. If the Flag is set, the processon can accept interrupts. if is cleared, interrupts are disabled.

* Usage:

* Set to enable interrupts.

* Cleared to disable interrupts.

Ex. When the IF Flag is set, extern/ hardware interrupts can interrupt the processon, If it is cleared, the processon ignores interrupt requests.

6. Over Flow Flag (OF).

* Bit : 011

*The Overflow Flag is set when the

signed result of an arithmetic operation exceeds the allowable range. It indicates that the result cannot be represented correctly with the given number of bits in a signed integer.

* Usage:

✓ Set if an overflow occurs in signed arithmetic operations.

Ex: In ADD AX, BX if the sum of two positive numbers results in a negative value, the OF flag will be set

" The End "