Victoria University of Bangladesh.

MD. Al AMIN

ID: 2121210041

Course: CSE-223 [Digital Electronic on Pulse Technique]

Dept of CSE/CSIT

Final Assessment - Fall 2024

Answer to the Question NO 1 (A).

A master-slave flip flop is a type of sequential circuit that consists of two flip-flops connected in series- one acting as the master and the other as the slave. This setup help in eliminating race conditions and ensures stable data transfer.

When the clock is High, the masthe flip flop is active.

Ex:

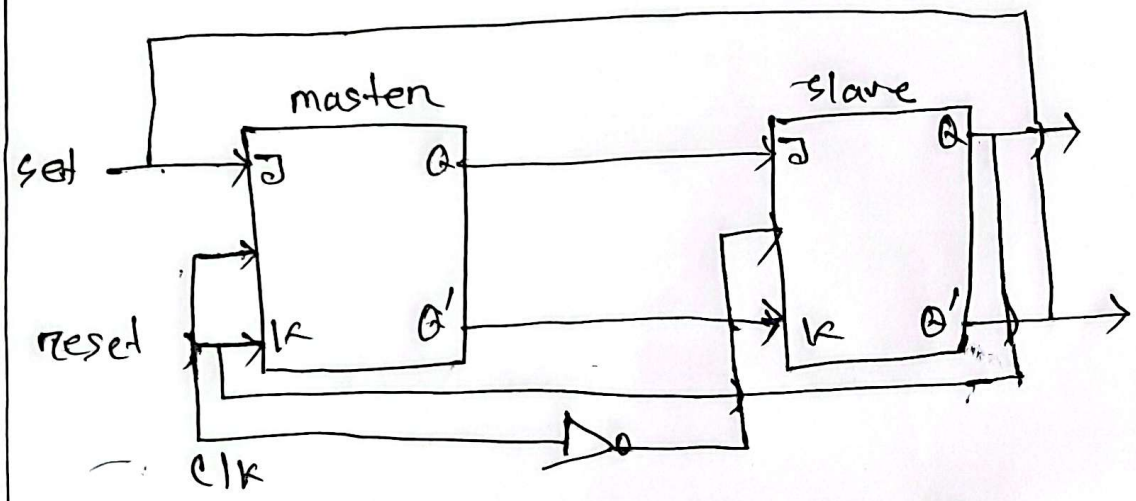
A flip-flop can be implemented as a master slave flip-flop using two flip-flops. The master flip-flop take inputs J and K.

Answer to the Question 1 (B).

In JK Flip Flop when both the inputs a CLK set to 1 for a long time then Q output toggle until the CLK is 1. Thus the uncertain output can produce.

Explination.

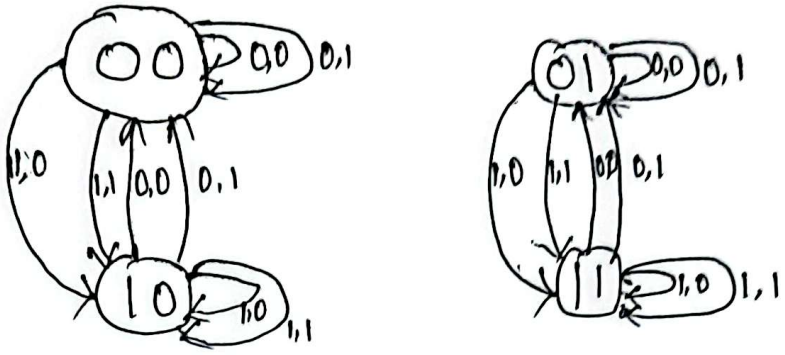
The master slave flip flop is constructed by combining two JK flip flops. These flip flops are connected in a series configuration.



Master-Slave JK Flip-Flop.

When the clock pulse is true the slave flip flop will be in the isolated state. The flip flop will be disabled and Q remains unchange when both the inputs of the JK flip flop set 0.

Answer to the Question No- 2(A).



Steps.

① Identify the states are represented by (A,B) pair.

Possible states : 00, 01, 10, 11

② Determine transitions : For each input (x, y) check how the state changes.

③ Draw circles for Each state label them as :

state 00
state 01
state 10
state 11

4. Draw directed Arrows for transition.

5. Include output values :

Each transition can be labeled with "x y/z where z is the output.

Answer to the Question NO - 3(A)

The MC74HC589A device consists of an 8-bit storage latch which feed parallel data to an 8 bit shift register. Data can also be loaded serially.

Features:

(I) Output drive capability 15 LSTTL Loads.

(II) Outputs Directly Interface to CMOS, NMOS and TTL

(III) Low input current : 1 μA.

(IV) Chip complexity: 526 FETs or 131.5 Gates.

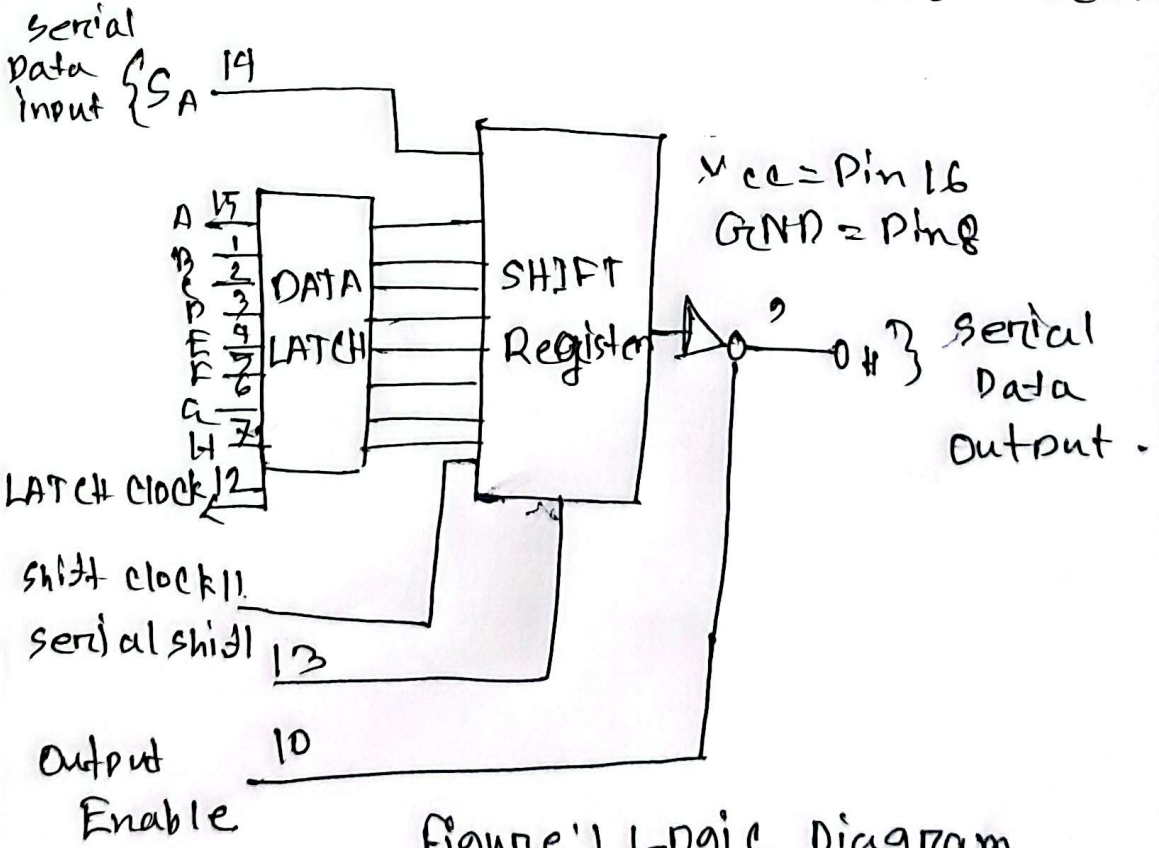
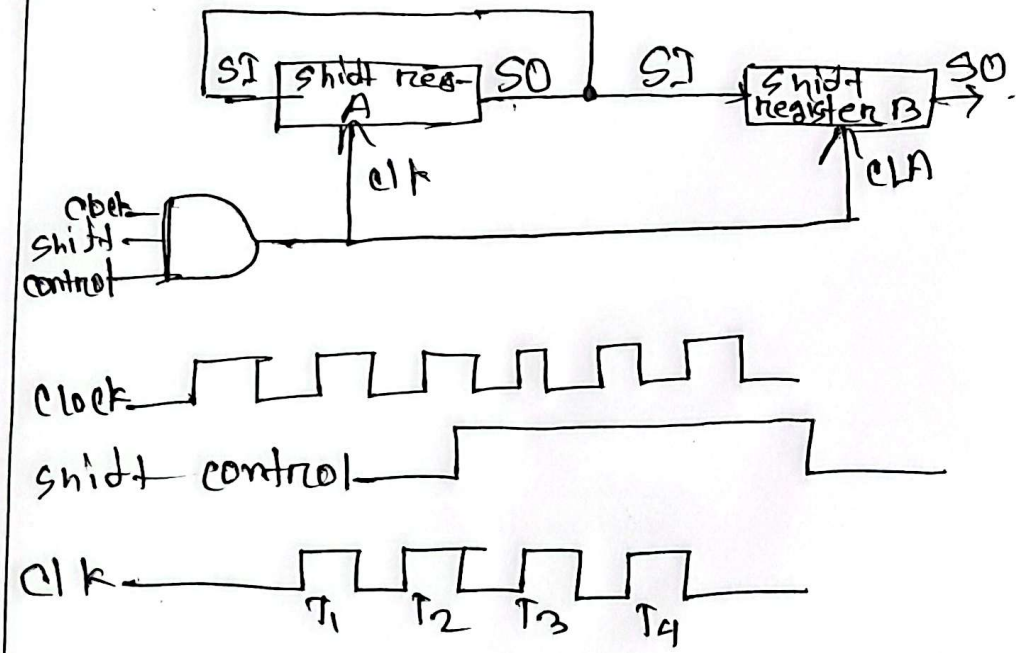


Figure: 1 Logic Diagram.

Answer to the Question NO-3(B).

Serial transfer:

A digital system is said to operate in a serial mode when information is transferred and manipulated one bit at a time.



The serial output (SO) of register A is connected to the serial input (SI) of register B. To prevent the loss of information.

D

Timing Pulse	Shift register A	Shift register B
Initial value	1 0 1 1	0 0 1 0
After T_1	1 1 0 1	1 0 0 1
After T_2	1 1 1 0	1 1 0 0
After T_3	0 1 1 0	0 1 1 0
After T_4	1 0 1 1	1 0 1 1