ID: 211608002 1
NAME: Ghulam Forhanul Bashar

Mid Term Examination
Summer 2024.

Date: 23 August 2024
Program: BSc in CSE
course code: CSE 427
course title: VLSI Design

Dept of CSE/CSIT
Victoria University
Bangladesh.

Ans 1) a) The floor planning for a standard cell based

1) Partitioning: Divide the design into smaller blocks for easier management and optimization.

2) Block Placement: Arrange blocks to minimize inter-connection lengths, considering I/O pads, power and clock distribution.

3) Power Planning: Design power rings, straps and grids to ensure stable power across the chip

4) I/O Placement: Position I/O pads around the chip periphery to reduce signal delay and crosstalk.

5) Clock planning: Ensure balanced clock distribution with minimal skew using a clock tree or grid

6) Routing channels: Allocate channels for interconnects avoiding congestion

7) Area optimization: Minimize chip area while meeting performance and power goals.

8) Aspect Ratio: Maintain a suitable aspect ratio for manufacturability.

9) DRC checks: Ensure compliance with design rules for physical constraints.

Ans 1) b) The linear delay model in VLSI is a simplified to estimate the delay of a digital circuit. It assumes that the delay the delay through a gate is a linear function of a capactive load it drives and the intrinsic delay of the gate itself. The model is defined by the equation

Delay = Intrinsic Delay + (slope × load capacitance)

- Intrinsic Delay: The inherent delay of the gate with no load
- Slope (or drive resistance): Represent how much the delay increases with an increase in load capacitance.
- Load capacitance: The total capacitance driven by the gate including wire capacitance and the input capacitance of the next gate(s)

This model provides a quick and straight forward way to estimate delay.

Aus 1) c) The equation of voltage dependance especially in the content of MOSFET explains how the current flowing through the transistor depends on the voltages applied to it, in the saturation region, where the MOSFET is fully on and acting like a constant current source, the drain current I_D is given by

$$I_D = \frac{1}{2} u_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS})$$

Here • u_n is the mobility of electrons in the channel which affects how easily they move.

• C_{ox} is the capacitance of the oxide layer, influencing how much the gate voltage can control the channel.

• W/L is the width to length ratio of the MOSFETs channels determining how much current can flow.

• V_{GS} is the gate to source voltage which controls the transistor. When V_{GS} is greater than the threshold voltage V_{th} the MOSFET turns on

• V_{th} is the threshold voltage the ~~minimum~~ minimum V_{GS} needed to create a conducting channel.

• λ represent the channel-length modulation, which accounts for the slight increase in current with increasing V_{DS} even in saturation.

Aus 2) a) Threshold voltage:

nMOS: $V_{th,n} = V_{FB,n} + \phi_s + \gamma \sqrt{\phi_s + V_{SB}}$

pMOS: $V_{th,p} = V_{FB,p} - \phi_s - \gamma \sqrt{\phi_s - V_{SB}}$

Critical voltage for fully on state For the transistor to be fully on ~~for nMOS~~ the gate source voltage V_{GS} must be greater than the threshold voltage for an nMOS transistor ($V_{GS} > V_{th,n}$) and for pMOS transistor ($V_{GS} < V_{th,p}$).

Ans 2) b) As we know change in threshold voltage due to the body effect is given by

$$\Delta V_{th} = V\left(\sqrt{\phi_s + V_{SB}} - \sqrt{\phi_s}\right)$$

Here $\phi_s = 2 \times \phi_F$ [$\because \phi_F$ = Fermi potential]

and $\phi_F = \frac{KT}{q} \ln\left(\frac{N_a}{n_i}\right)$

$$= \frac{8.617 \times 10^{-5} \times 300}{1.6 \times 10^{-19}} \ln\left(\frac{8 \times 10^{10}}{1.5 \times 10^{10}}\right)$$

[$K = 8.617 \times 10^{-5}$ eV/K
$T = 300$K
$q = 1.6 \times 10^{-19}$ C
$N_a = 8 \times 10^{10}$ cm^{-3}
$n_i \approx 1.5 \times 10^{10}$ cm^{-3}]

$$\phi_F \approx \frac{0.0259}{2.6 \times 10^{-19}} \times \ln(5.33)$$

$$\approx 0.0259 \times \ln(5.33)$$

$$\approx 0.0259 \times 1.675$$

$$\approx 0.0434 V$$

$\therefore \phi_s = 2\phi_F \approx 0.0868 V$

The body coefficient $V = \sqrt{\frac{2\varepsilon_s N_a}{C_{ox}}}$

$\neq$

Here $\varepsilon_s \approx 11.7 \times \varepsilon_0$
$\approx 11.7 \times 8.854 \times 10^{-14}$

and $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

for 65 nm process lets assume $t_{ox} \approx 2$ nm $= 2 \times 10^{-7}$
and $\varepsilon_{ox} \approx 3.45 \times 10^{-13}$ F/cm.

So $C_{ox} = \frac{3.45 \times 10^{-13}}{2 \times 10^{-7}}$.

$\approx 1.725 \times 10^{-6}$ F/cm^2

Now $V = \sqrt{\frac{2 \times 1.6 \times 10^{-19} \times 11.7 \times 8.854 \times 10^{-14} \times 8 \times 10^{10}}{1.725 \times 10^{-6}}}$

$V \approx \sqrt{\frac{2.19 \times 10^{-32}}{1.725 \times 10^{-6}} \times 8 \times 10^{10}}$

$V \approx 3.56 \times 10^{-13} \times 8 \times 10^{10}$

$V \approx 0.0285 V^{1/2}$

Ans 2)b)

Now

Threshold voltage change

$$\Delta V_{th} = 0.0285 \times (\sqrt{0.0868 + 0.6} - \sqrt{0.0868})$$

$$\Delta V_{th} = 0.0285 \times (\sqrt{0.6868} - \sqrt{0.0868})$$

$$\Delta V_{th} = 0.0285 \times (0.829 - 0.2945)$$

$$\Delta V_{th} \approx 0.0152 V$$

Here $V_{th0} = 0.3V$

So threshold voltage is

$$V_{th} = V_{th0} + \Delta V_{th}$$

$$V_{th} \approx 0.3V + 0.0152V$$

$$\approx 0.3152V$$

So when the source is at 0.6V instead of 0V, the threshold voltage of the nMOS transistor increases by approximately 0.0152V and making the new threshold voltage $V_{th} \approx 0.3152V$ at room temperature.