Name : Abdullah Bin Noman Tabid

Student ID : 2120180031

Counse Code : CSE-313

Counse Title : Computere ~~Architect~~ Architecture

"final Assessment"

1

Ans to the Q No 1

(a)

The IBM z Enterprise EC12 channel subsystem structure -

(1) Improved total system capacity in a 120 core design -

(a) Optimization and scale improvements starting at the core.

(b) Massive scalability for secure data serving and transaction processing and large-scale consolidation.

(2) Hexa-core 5.5 GHz processor chips design with a boost in performance for all workloads -

(a) Second-generation out-of-order design.

(b) Larger cache sizes to optimize data serving environments.

(3) New Crypto Express 4S cryptographic adapter.

(a) Support for the PCIe I/O drawer configuration.

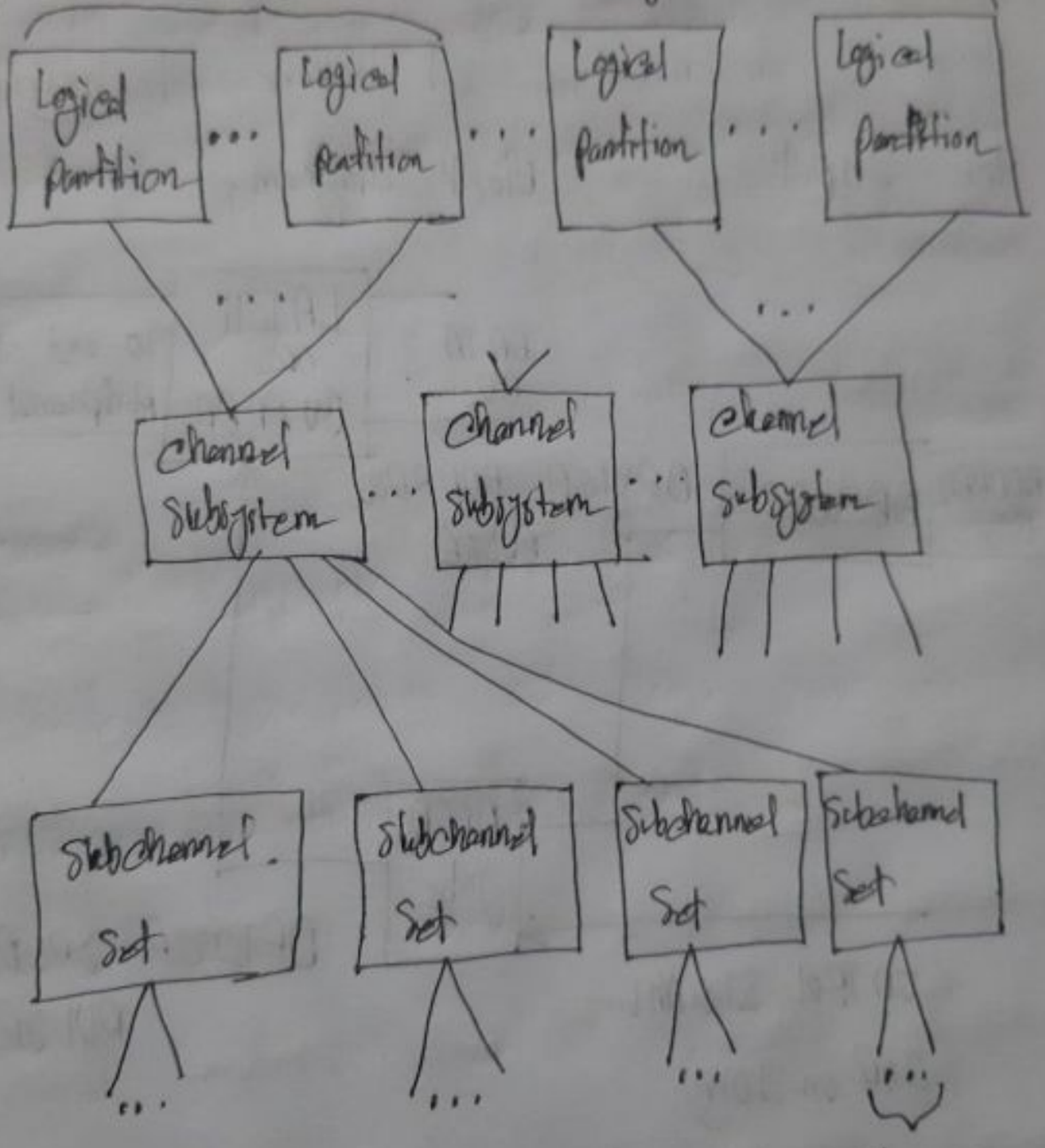
(b) Support for digital signatures with new PKCS #11.

(c) Support for American Express EMV (Europay, Mastercard, Visa) cards.

(4) New IBM z Aware cutting-edge pattern recognition analytics for fast insight into system health

d 85 Partition per system

d 15 Partition per channel subsystem



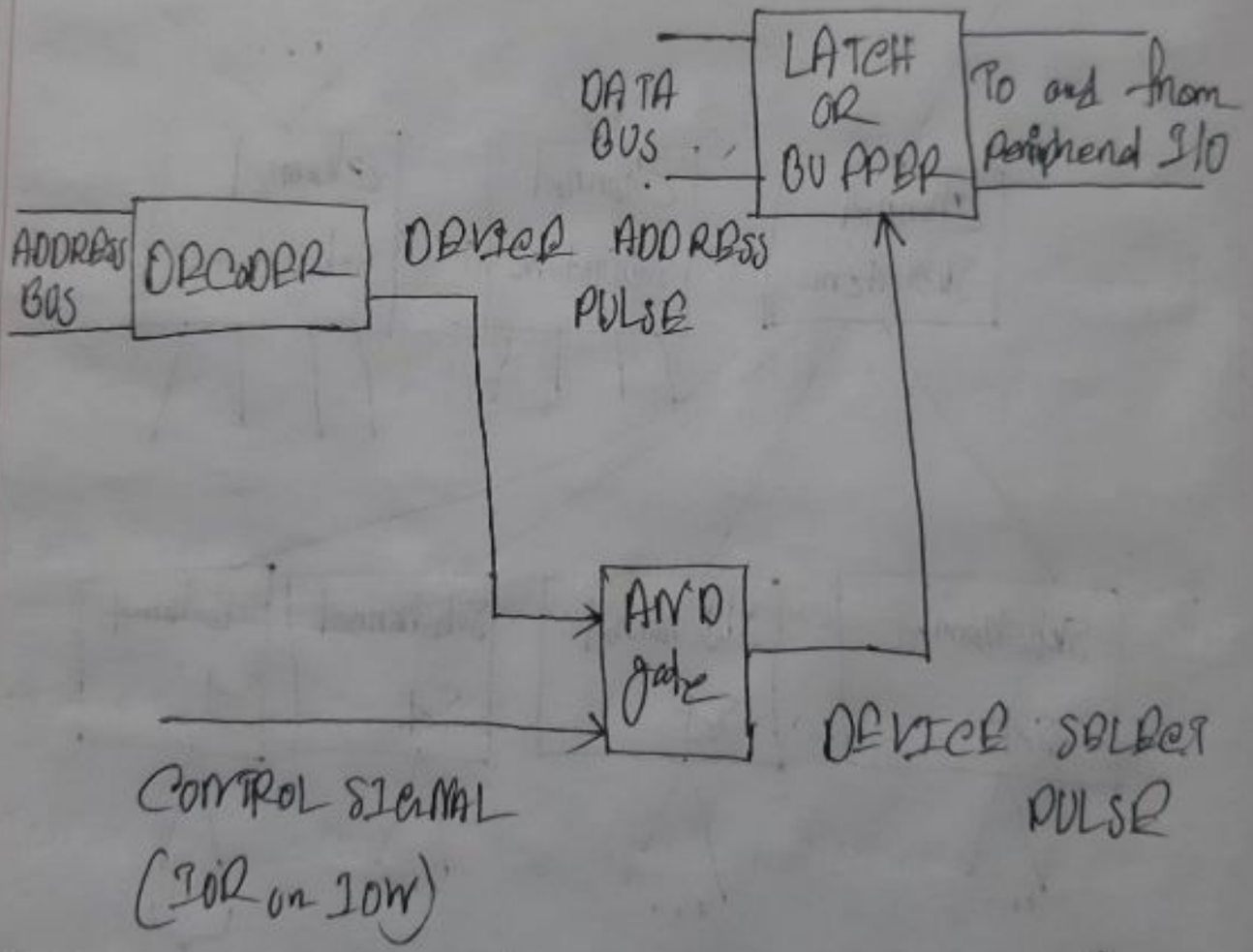
cpto 64k channels per subchannel set

Figure: IBM 213 I/O channel structure.

Ans to the Q No 1

(a)

Here is description of three techniques for Input of a Block diagram-



A simple block diagram of I/O interface

The basic input output device is a set

of three-state buffers. The basic output device is consisting of data latches. The term IN presents for moving data from term OUT presents for moving data out of the microprocessor to the I/O device. The three-state buffers are used to construct an 8-bit input port. The external TTL logic data are connected to the input of the buffers. The output of the buffers connected to the data bus.

Ans to the Q. No 2

(a)

Cache memory: Cache memory, supplementary memory system that temporarily stores frequently used instructions and data for quicker processing by the central processing unit (CPU) of a computer.

Main memory: Main memory is the primary internal work space in the computer, commonly known as RAM (random access memory). Specifications such as 4GB, 8GB, 12GB and 16GB almost always

Refers to the capacity of RAM.

Ans to the Q. No : Q2

(b)

Logical Cache: By using logical record cache definition, we can define the attributes of a logical record cache and manage a cache by using only z/~~TPF~~ TPF commands.

A logical record cache definition is a persistent description of a logical record cache. The cache definition specifies the name and attributes that are used to create the cache.

physical Cache: physical cache memory is a chip-based computer component that makes retrieving data from the computer's memory more efficient. It acts as a temporary storage area that the computer's processor can retrieve data from easily.

9

Ans to the Q. No 3

(a)

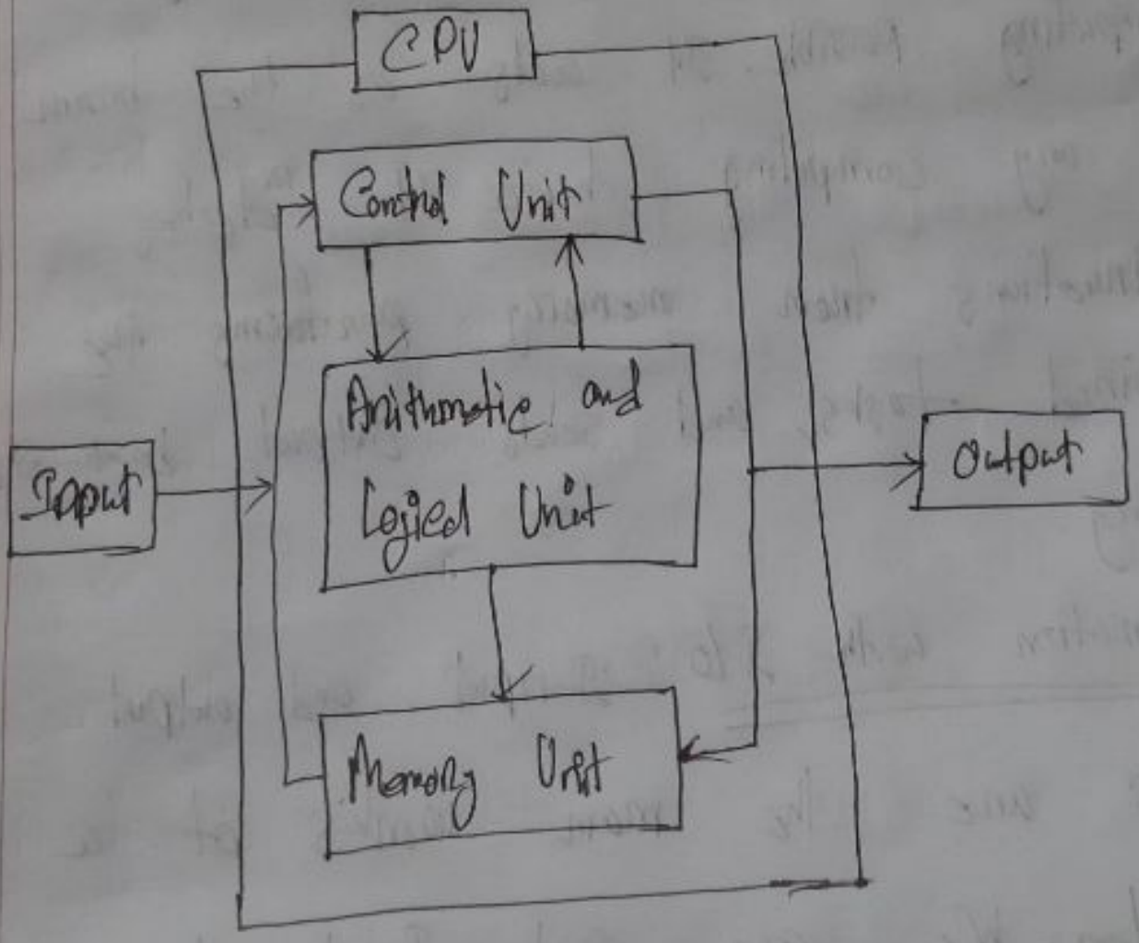


Figure: Block diagram of a C.P.U.

Interaction with the main memory:

The CPU is the primary component that processes the signals and makes computing possible. It acts as the brain of any computing device. It fetches instructions from memory performs the required tasks, and sends output back to memory.

Interaction with I/O: Input and output signals are the main works of a computer. We can set Input to a C.P.U and ~~can't~~ can get output signals. That's the main process.

Ans to the Q No 3

(b)

There aren't really official names for most forms of x86 addressing modes. They all have the form [base + index * scale + disp8 / disp32] (or a subset of that), except any 1 or 2 components of for 64 bit RIP relative addressing.

Indirect addressing:

a) in direct addressing, the memory location of the operand is in the two / four bytes following the opcode.

(b) in indirect addressing, the memory location of a pointer to the operand is in the two/four bytes following the opcode.

for example, the following code jumps to the location pointed to by the two bytes at location 1000_{16}:

```
0123    JMP (1000H)
...
1000    67H
1001    45H
```

This jump transfers execution to the instruction found at location 4567.

Ans to the Q No 1

(b)

events occur: The device issues an interrupt signal to the processor. The processor finishes execution of the current instruction before responding to the interrupt. Also occurs -

① The device issues an interrupt signal to the processor.

② Processor finishes the execution of current instruction after responding to the interrupt.

③ Processor needs to save information to resume the current program at the

Point of interrupt.

④ <P> Minimum information required to save to resume the current program at the point of interrupt is only the status of the processon <[P>.