VICTORIA UNIVERSITY BANGLADESH

Assignment On

Course Name : Digital Logic Design

Course code : CSE-213

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Ans. to the Q.NO - 1(a)

* **Demultiplexer:**

* A demultiplexer is a devie that takes a single input line and routes it to one of several digital output line.

* We have 1×2, 1×4, 8×1 ... Demultiplexer.

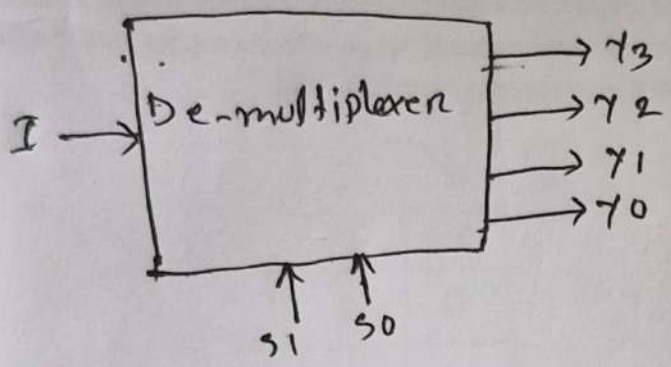

Fig:- 1 Block Diagram

selection input		output			
S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Fig:2 Truth table.

$Y_3 = S_1 S_0 I$

$Y_2 = S_1 S_0' I$

$Y_1 = S_1' S_0 I$

$Y_0 = S_1' S_0' I$

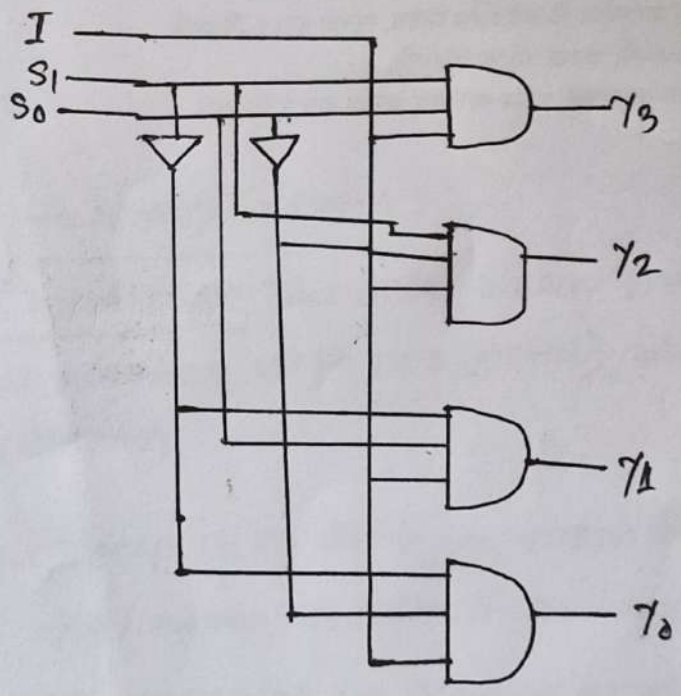

Fig-3 logic Diagram:

Ans. to the Q.NO-1 (b)

b An Encoder is a combinational circuit that performs the reverse operation of Decoder. it has maximum of 2^n input lines and 'n' output lines.

Octal to binary encoder Truth table:

Octal Digit		Binary		
		A_2	A_1	A_0
D_0	0	0	0	0
D_1	1	0	0	1
D_2	2	0	1	0
D_3	3	0	1	1
D_4	4	1	0	0
D_5	5	1	0	1
D_6	6	1	1	0
D_7	7	1	1	1

Fig- Truth table.

*Limitation of octal to binary Encoder:

① ~~Limitation~~ Limited input Range: The octal Binary Encoder can only convert octal number up to 177 (octal), which is equivalent to 128 (Binary).

② Error Detection: There is on Build-in error detetion mechanism in the octal Binary Encoder. If an invalid octal input is provided, the output may not be accured on may be incorrect etc.

Ans to the Q.No-2(a)

Q Decoder: A decoder is a circuit that changes a code into a set of signals. It is called a decoder because it does the reverse of encoding, But we will begin ~~out~~ our study of encoders and decoders with decoders because they are simpler to design.

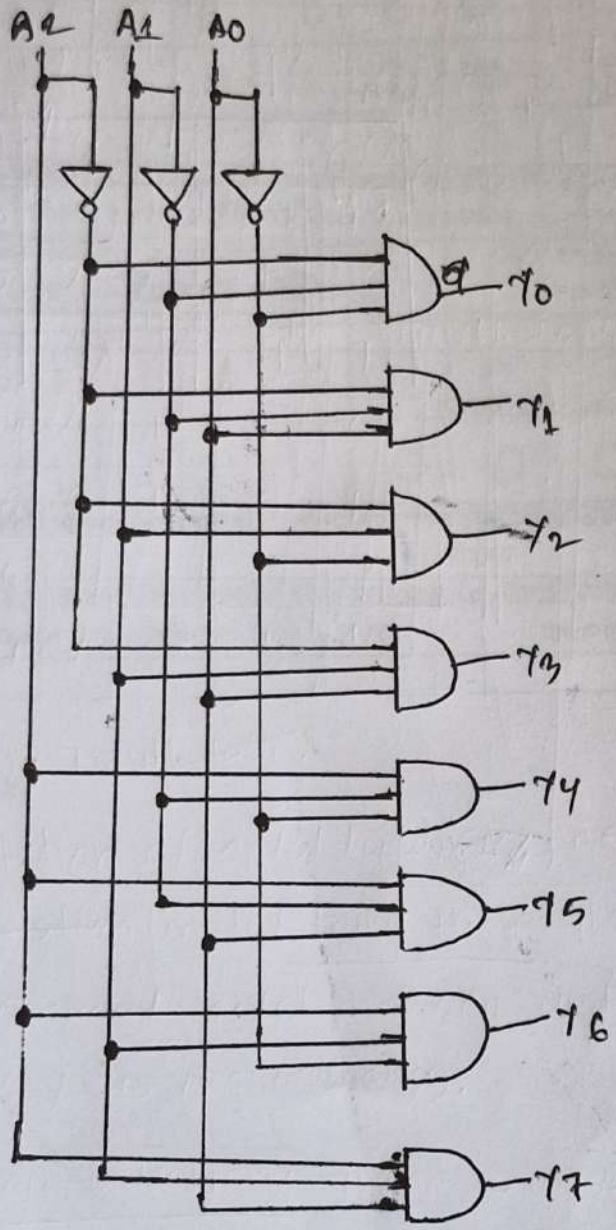

Fig: Logic Diagram. 3 to 8.

3 to 8 Truth Table:

Enable	Input			output							
E	A_2	A_1	A_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	x	x	x	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

Fig. 3 to 8 Truth table.

Ans. to the Q.NO-2(6)

* JK Flipflops: JK flipflop is a basiclly a gated SR flip-flop with the additional of a clock input circuitry that prevents the illegal or ~~indiva~~ invalid output condition that can occur when both inputs S and R are equal to logical level "1" Logic "0" no, "change" and "toggle". The symbol for a JK flip-flop is similar to that or an SR Bistable latch as seen in the pervious tutorial except for the additional of clock input.

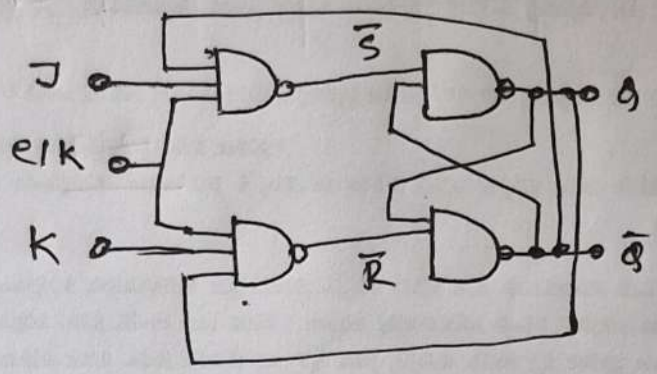

Fig: JK Flip-flop Logic Diagram.

The Truth Table for the JK Flip-Flop.

	Clock	Input		output		Description
	clk	J	K	Q	$\bar{Q}$	
Same for the SR Latch	x	0	0	1	0	memory No change
	x	0	0	0	1	
	↓	0	1	1	0	Reset Q>0
	x	0	1	0	1	
	↓	1	0	0	1	set Q>1
	x	1	0	1	0	
toggle section	↓	1	1	0	1	Toggle
	↓	1	1	1	0	

Fig: