VICTORIA UNIVERSITY BANGLADESH

Assignment On

Course Name : Digital Logic Design

Course code : CSE-213

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Answer to the question NO 2 (a)

Decoder: A decoder is a circuit that changes a code into a set of ~~sig~~ signals. It is called a decoder because it does the reverse of encoding. But we will begin our study of encoders and decoders with decoders because they they are simpler to design

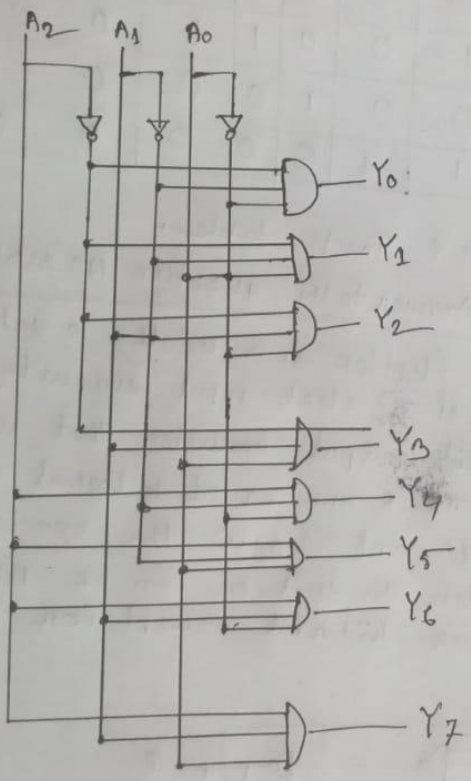

Fig: Logic Diagram. 3 to 8

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3 to 8 Truth Table

Enable	Input			Output							
E	A_2	A_1	A_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	x	x	x	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

Fig : 3 to 8 Truth table.

Answer to the question NO 2(b)

* JK Flipflops: JK flipflop is a basically a gated SR flip-flop with the additional of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs and R are equal to logical Level "1" Logic "0" no, "change" and "toggle" the symbol for a JK flip-flop is similar to that on an SR Bistable latch as seen in the perevious tutorial except for the additional of clock input

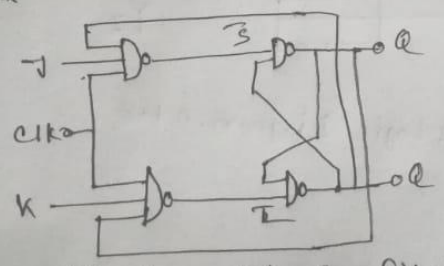

Fig: JK Flip-Fop Logic Diagram

 ~~flip.flop~~

Answer to the question NO: 1(a)

Demultiplexer:

* A demultiplexer is a devic that takes a single input line and routes it to one of several digital output line
* We have 1*2, 1*4, 8*1 ..... Demultiplexer.

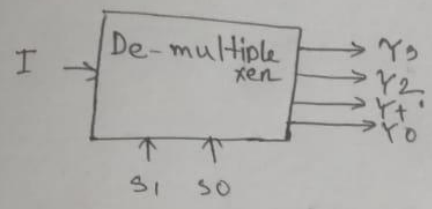

Fig-1 Block Diagram.

Input		output			
S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Fig 2: Truth table.

$Y_3 = S_1 S_0 I$

$Y_2 = S_1 S_0' I$

$Y_1 = S_1' S_0 I$

$Y_0 = S_1' S_0 I$

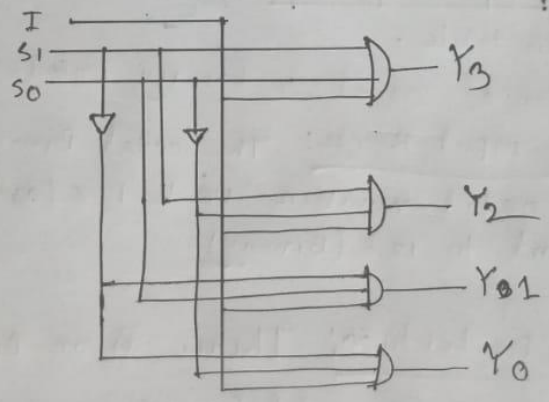

Fig - Logic Diagram

Answer to the question NO: 1 (b)

An encoder is a combinational circuit that performs the reverse operation of Decoder. It has maximum of 2^n input lines and 'n' output lines

octal to binary encoder Truth table

Octal Digit		Binary A_2	A_1	A_0
D_0	0	0	0	0
D_1	1	0	0	1
D_2	2	0	1	0
D_3	3	0	1	1
D_4	4	1	0	0
D_5	5	1	0	1
D_6	6	1	1	0
D_7	7	1	1	1

Fig - Truth table.

Limitation of octal to binary Encoder:

① Limited input Range: The octal Binary Encoder can only convert octal number up to 177 (octal), which is equivalent to 128 (Binary)

② Error Detection: There is on Build-in error detetion mechanism in the octal Binary encoder. If an invalid octal input is provided, the output may not be accurned or may be incorned etc