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Course Code : CSE-223

Course Title : Digital Electronics and Pulse Technique

"Final Assessment"

1

Ans to the Q No -1

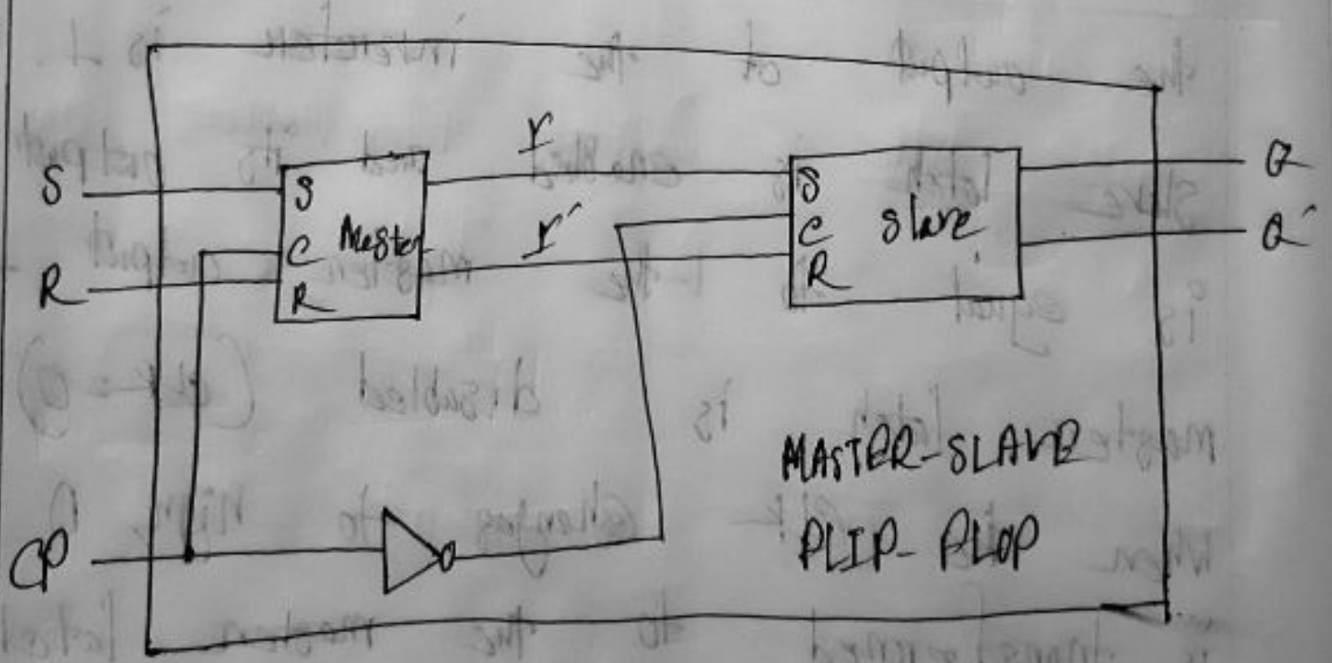
(a)

MASTER & SLAVE FLIP-FLOPS:

The circuit samples the D input and changes its output at the negative edge of the clock, CLK. When the clock is 0, the output of the inverter is 1. The slave latch is enabled and its output Q is equal to the master output Y. The master latch is disabled (CLK = 0). When the CLK changes to high, D input is transferred to the master latch. The slave remains disabled as long as CLK is low. Any change in the

input changes Y, but not Q. The output of the flip flop can change when CLK makes a transition; 1 → 0.

☐ Master Slave SR flip-flop (negative edge triggered) -

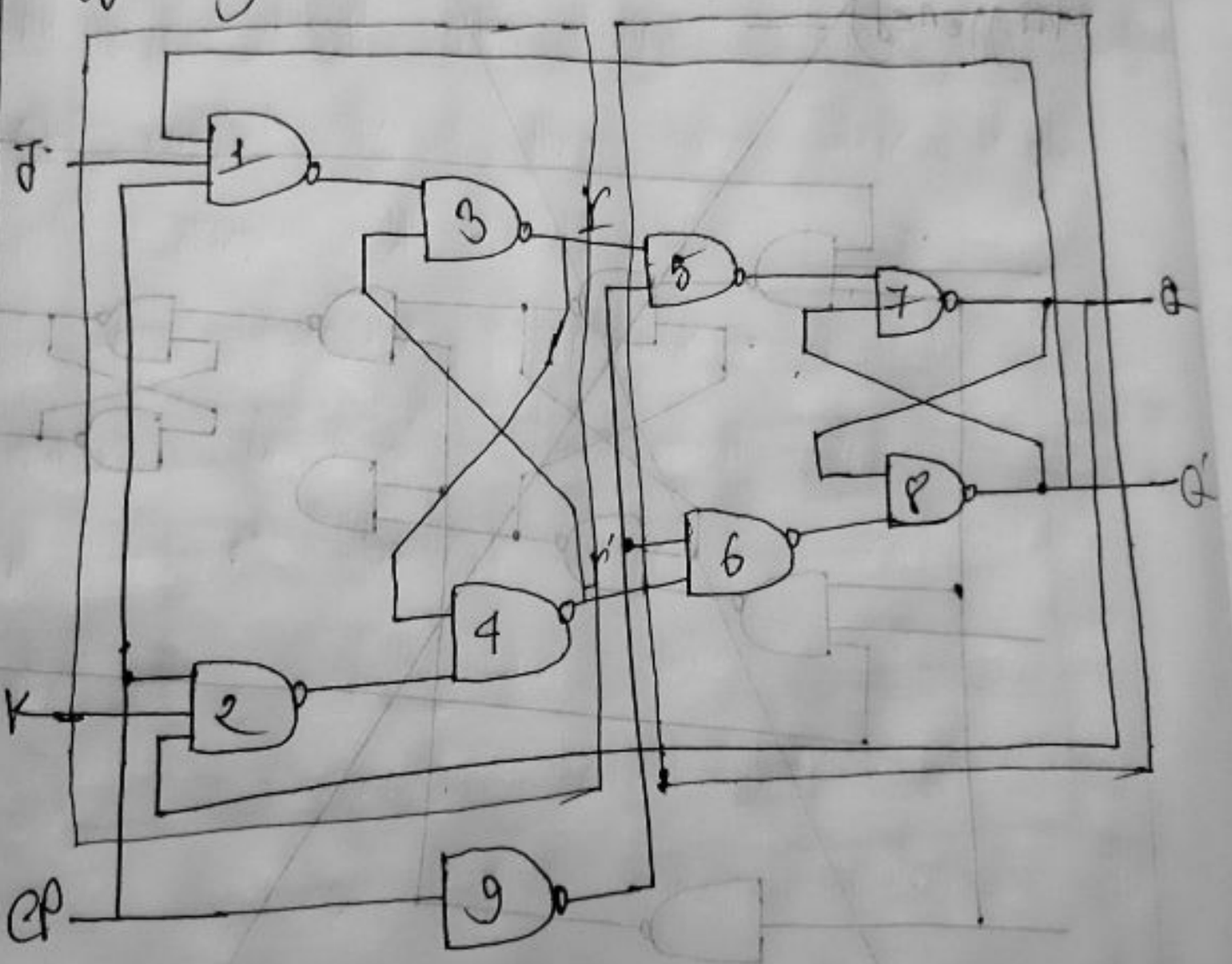


3

Ans to the Q No 1

(D)

Master Slave JK Flip - Flop (negative edge triggered) —



The circuit samples the J input and changes its output at the negative edge of the clock, CP.
When the clock is 0, the output of the inverter is 1. The slave latch is enabled. AND gate 5, 6, 7, 8 is enabled. These gates which means slave's output ~~it~~ is equal to the master output P.
The master latch gate No. 1, 2, 3, 4 is disable when (CP=0).
When the CP changes to high, J input is transferred to the master latch. The slave remains disabled as long as CP is low. Any change in the input changes

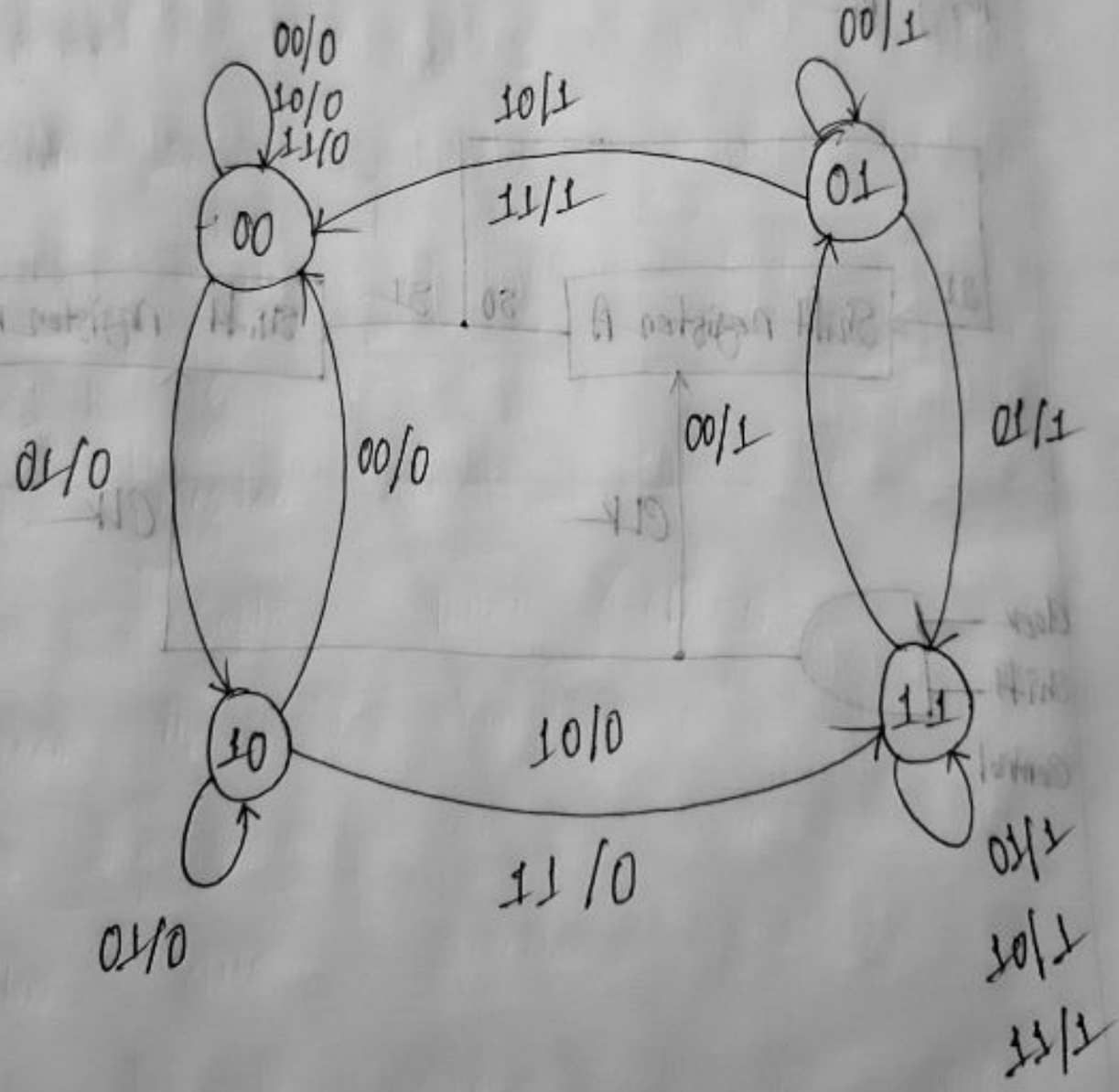
K but not Q for J input.

Similarly for K input circuit changes output for the negative edge of the clock, CP. When the CP is 0, the ~~out~~ output is 1. Then the slave latch is enabled and its output Q' is equal to the master output Y'. For CP=0 the master latch is disabled. When CP is high the K input is sent into master latch but when CP is low slave remains disabled. When CP is high the K input when changes the Y' is being changed for this, but not Q'.

Ans to the Q No 2

(a)

Following state diagram is

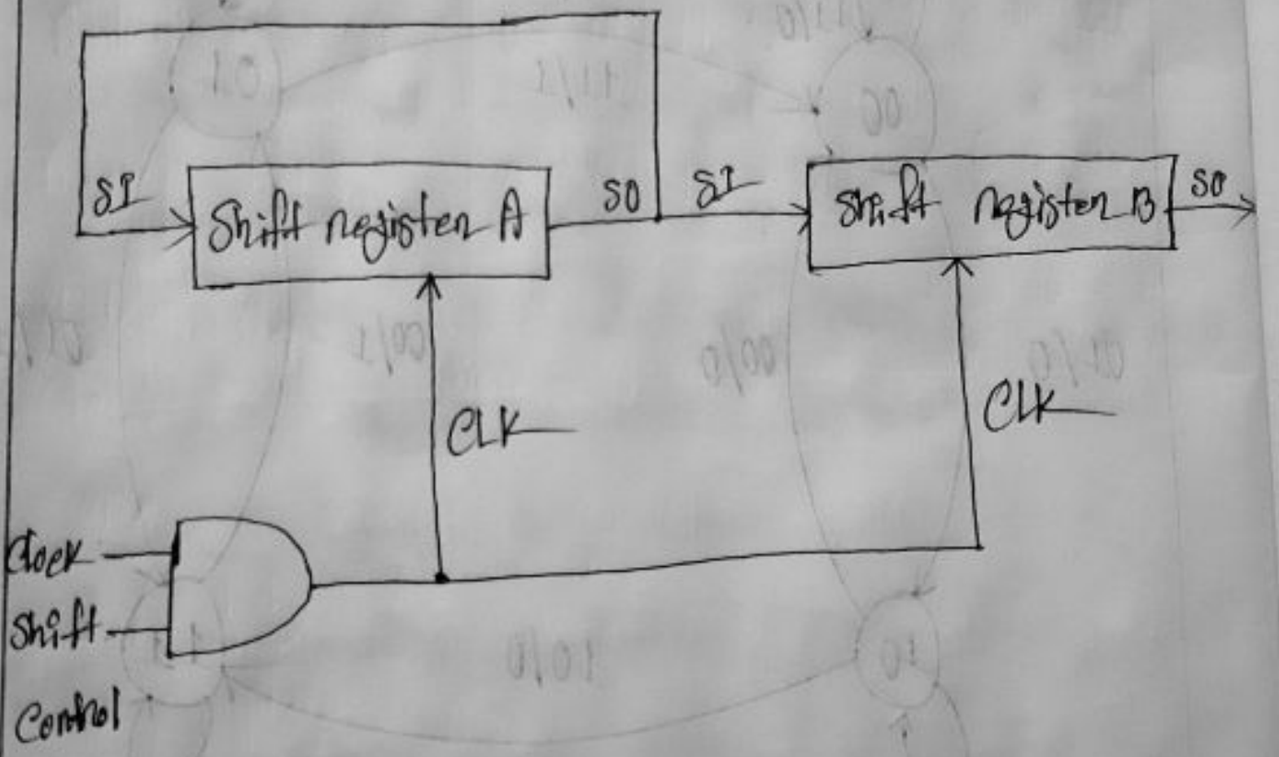


7

Ans to the Q. No 3

(b)

Serial Transfer from register Reg A to Reg B -



Serial - Transfer Example -

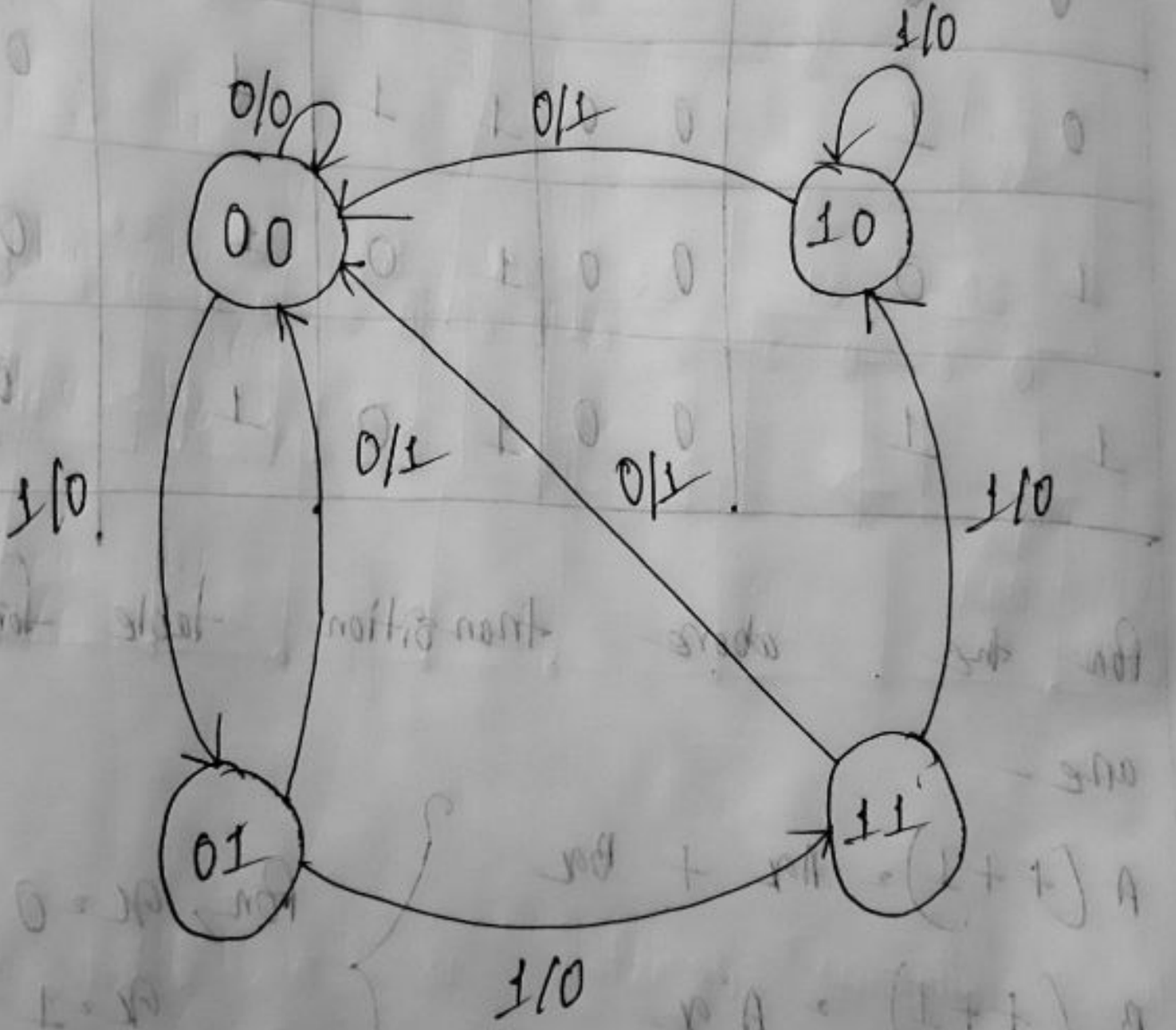
Timing Pulse	Shift Register A	Shift Register B
Initial Value	1 0 1 1	0 0 1 0
After T_1	1 1 0 1	1 0 0 1
After T_2	1 1 1 0	1 1 0 0
After T_3	0 1 1 1	0 1 1 0
After T_4	1 0 1 1	1 0 1 1

9

Ans to the Q No 4

(a)

State Diagram for the following question.



Present State		Next State			Output	
		$x=0$		$x=1$	$x=0$	$x=1$
A	B	A	B	A B	y	y
0	0	0	0	0 1	0	0
0	1	0	0	1 1	1	0
1	0	0	0	1 0	1	0
1	1	0	0	1 0	1	0

For the above transition table formulas are

$A(t+1) = Ax + Bx$

$B(t+1) = A'x$

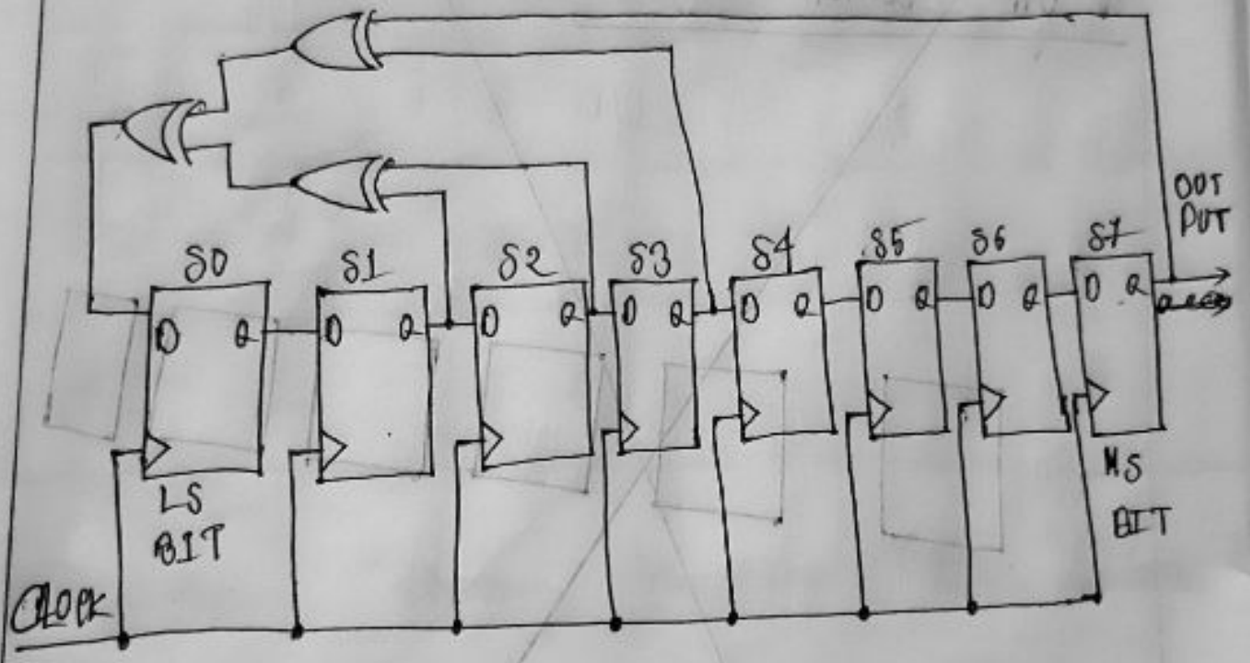
$y(t) = (A+B)x'$

} For, $x=0$, $x=1$

Ans to the Q No 3

(a)

8-bit serial register -



The following register is a 8-bit serial register. There is clock for every cell. There is X-OR gate for the register. Cell names are S0, S1, S2, S3, S4, S5, S6,

57. All the cells are connected via a protocol which source to destination register. For every cell there is input which is called D and output is called Q. By combining all the functions the 8-bit serial register is built.

If the clock is disabled the registers turns to off mode. There is X-OR functions for the following gate.