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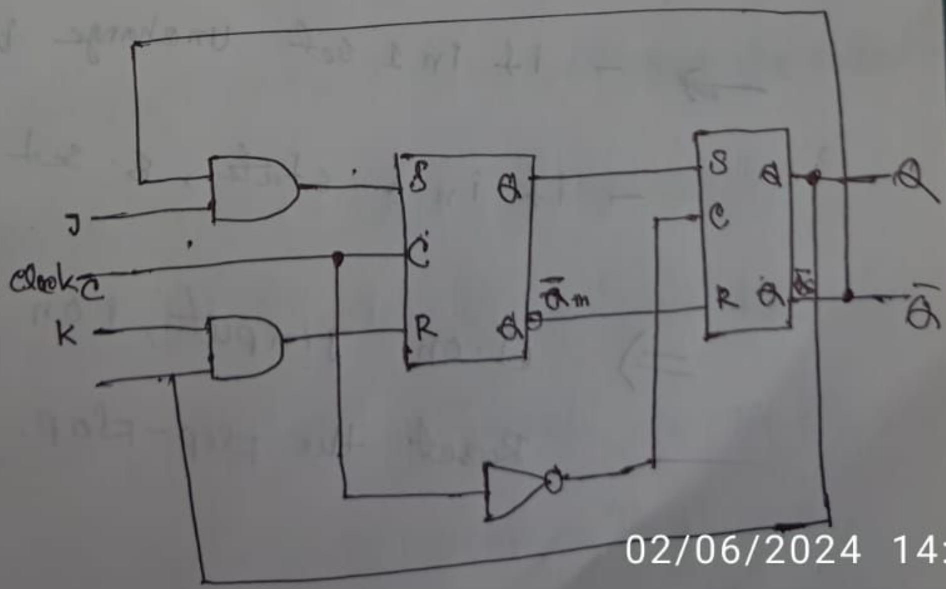
Course - Digital Electronics And pulse Technique.

Code - CSE-223.

Answer to the Question No- 1 (a)

(a) Ans: Master & slave flip-flop: A master - Slave flip-flope is Made by Connecting two JK flip-flops in a series Configuration in which one acts as the master and Another as a slave. The two inputs of Slave are Connected with the Output of the Master flip-flop. Furthermore, the master flip-flop input are fed back by output of the Slave flip-flop.

Example:



⇒ Assum in 1 - state, C = 0, J = k = 1.

- Due to feedback, the Output of the J-gate is 0,
  Out put of k-gate is 1.
- if clock is change to C = 1 then master is Reset.

⇒ Assum in 0 - state, C = 0, J = k = 1.

- Due to feedback. the Out put of the J-gate is 1
  out put of k gate is 0.
- if clock is change to C = 1 then master i's set

⇒ 1 on J input line, 0 on k input line sets the Flip-Flop,

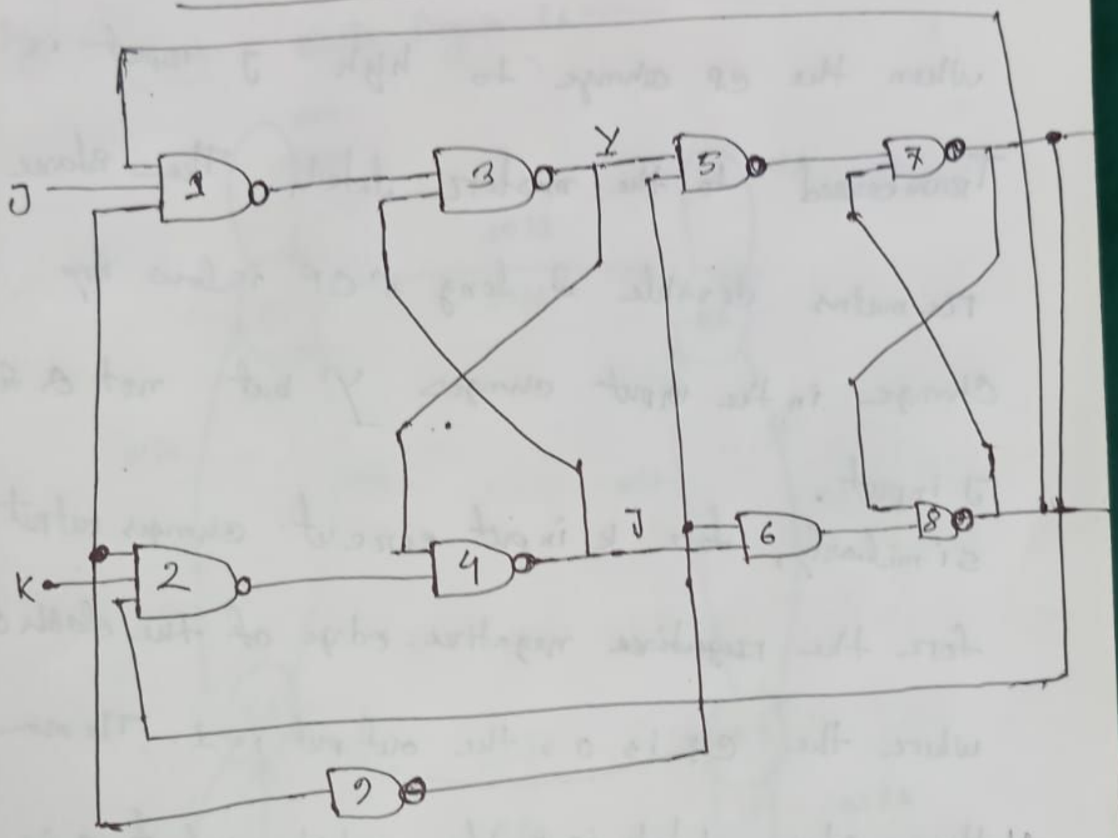
- if in 1 set unchange b/c S, R, set to 0.
- if in 0- state, S. set to 1, R set to 0.

⇒ 0 on J input, 1 on k input line.
Reset the Flip-Flop.

02/06/2024 14:26

① ⓑ Answer:

⇒ Master - slave Flip-flop using JK FF:



The circuit samples the J input and changes its output of the Negative edge of the clock, CP.

when the clock is 0 the out put of the Inverter is 1. The slave latch is Enable.

AND gate 5, 6, 7, 8, is enable. These gates which means slave's output is equal to the

P.T.O

Master output Y. The master latch gate

No 1, 2, 3, 4. is disable to when (CP-0)

when the CP change to high J input is

Transferred to the master latch. The slave

remains disable & long CP is low any

Change in the input changes Y but not Q for

J input.

similarly, for k input circuit changes output

for the ~~negative~~ negative. edge of the clock CP

where the CP is 0, the output is 1. Then

the slave latch is Enable and its output Q is

~~e tar~~ equal to the master output Y for CP=0

The master latch when is low slave remains

disable when CP is high the K input when

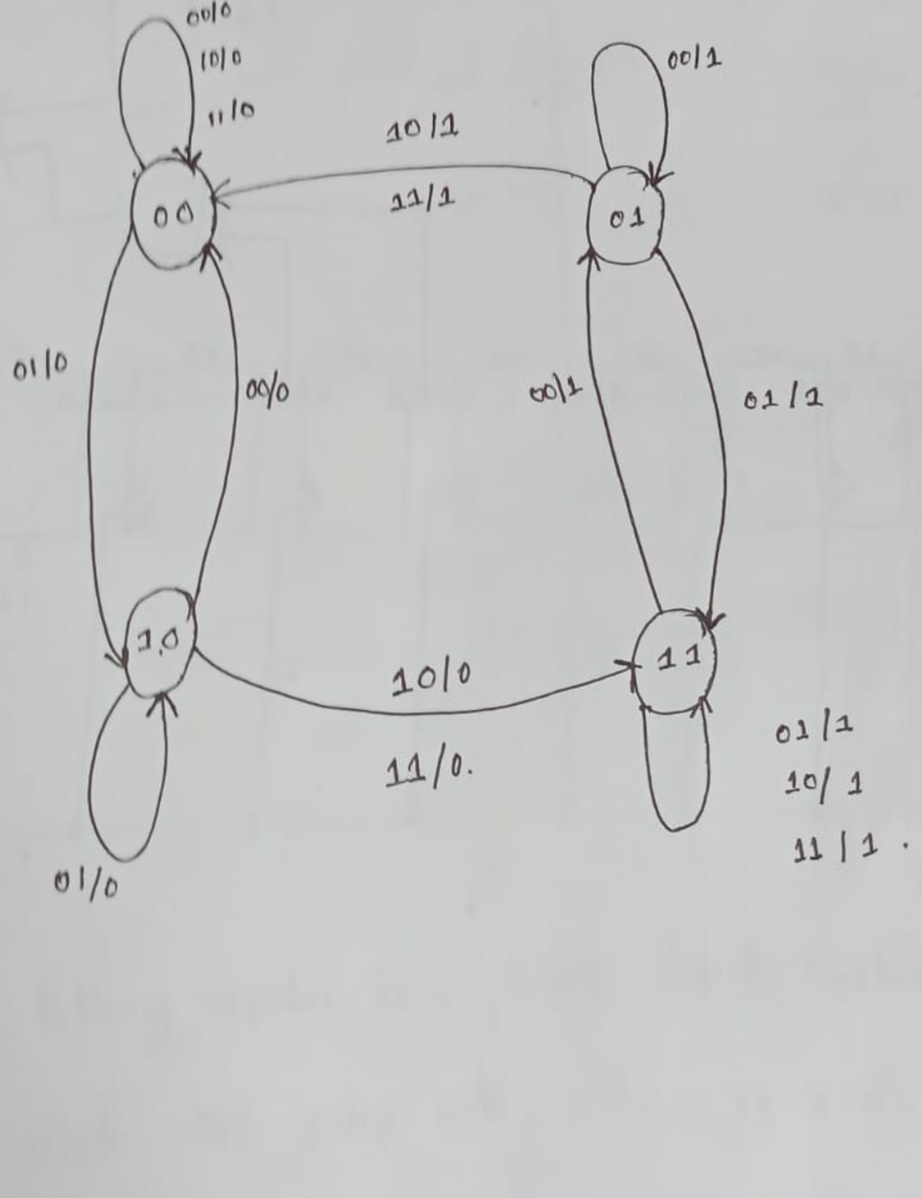
change the Y is being change for this but

not Q.

02/06/2024 14:27

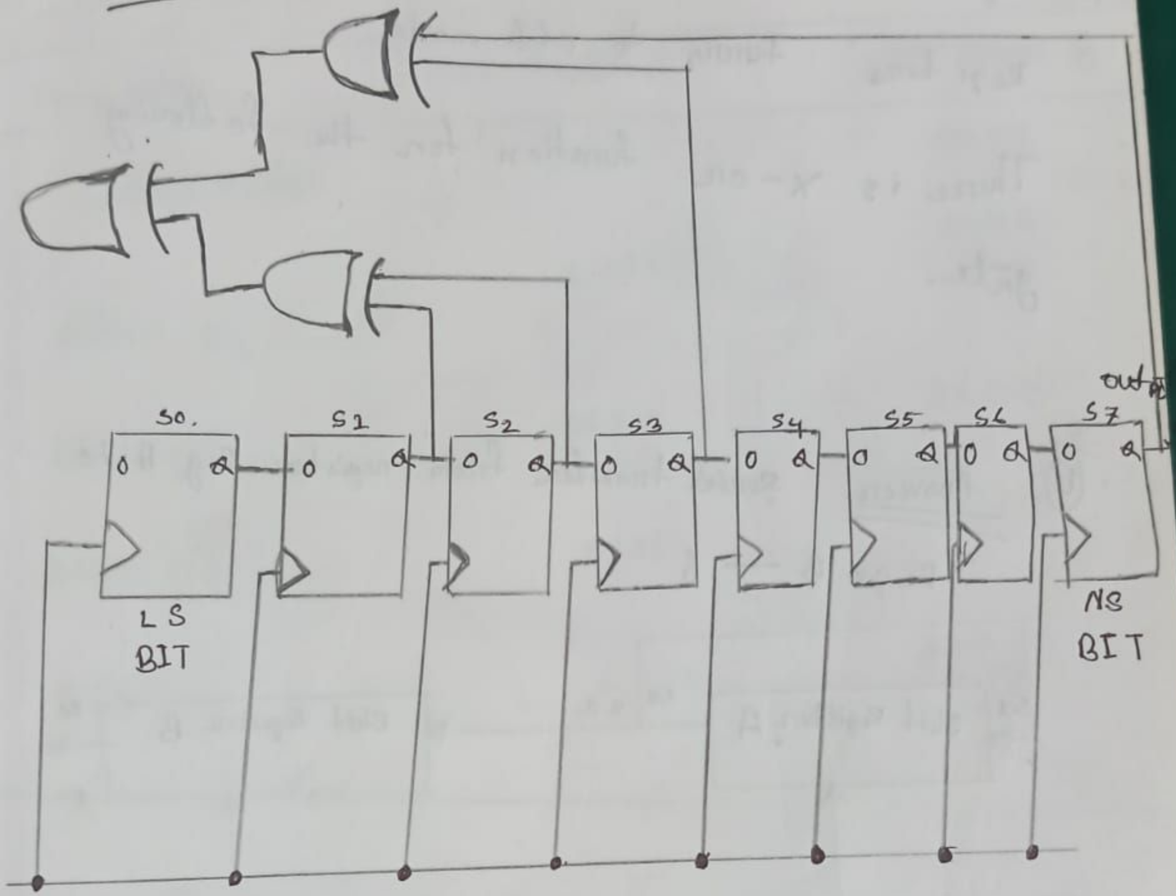
Answer to the Qustion No - 2

2(a) Answer: State Diagram is —



Answer to the Qustion No-3

(8) Answer:



Clock.

The following register is a 8-bit serial register. There is clock for every cell. There is X-OR gate for the register cell names are S0, S1 ... S7

All the cell are connected via a protocol which source to Destination register for energy cell there is input which is

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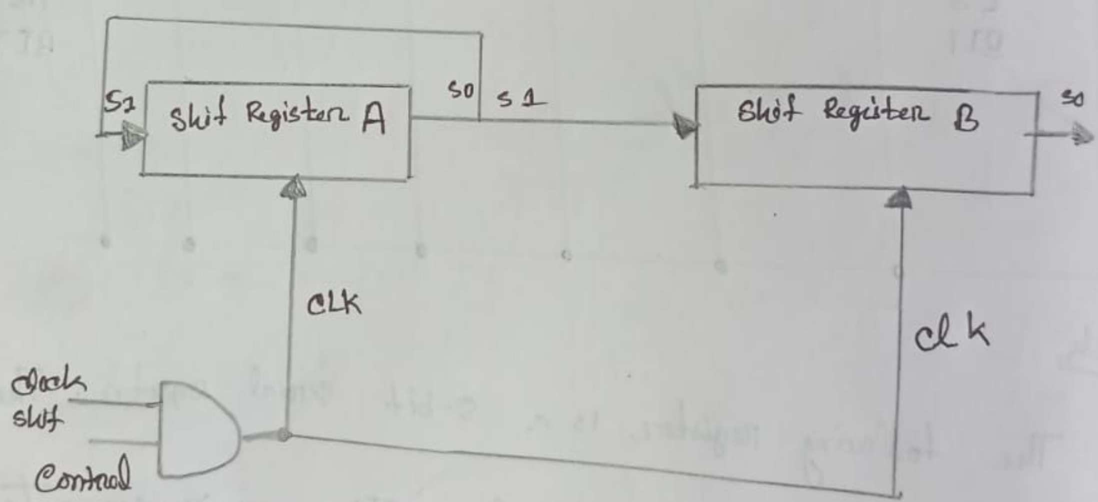
called 0 and out put is called Q. By combining all the functions the 8-bit serial register is built. if the clock is disabled the Registers turns to off mode.

There is X-OR function for the following gate.

3/(b) **Answer:** Serial transfer from register Reg A to Reg B — 8



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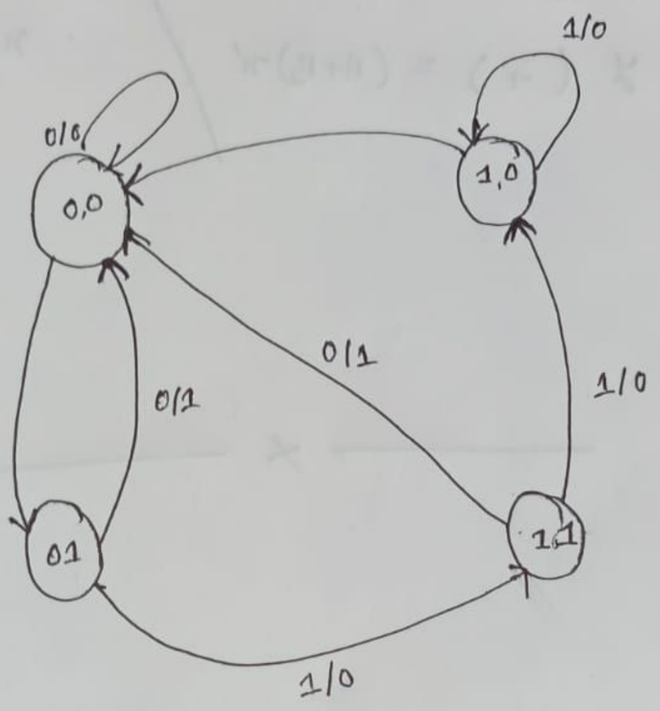
⇒ Serial transfer – Example –

Timing pulse	Shift Register A	Shift register B
Initial value	1011	0010
After P_1	1101	1001
After P_2	1110	1100
After P_3	0111	0110
After P_4	1011	1011

02/06/2024 14:27

Answer to the Question No - 4

(a) Answer: Diagram for the given table -



present state		next state		output	
		$x=0$	$x=1$	$x=0$	$x=1$
A	B	A B	A B	y	y.
0	0	0 0	0 1	0	0
0	1	0 0	1 1	1	0
1	0	0 0	1 0	1	0
1	1	0 0	1 0	1	0

For the above transition table formulas are

Ans

$$\left.\begin{aligned} A(t+1) &= Ax + Bx \\ B(t+1) &= A'x \\ y(t) &= (A+B)x' \end{aligned}\right\} \text{for } x=0,\ x=1.$$