Victoria University of Bangladesh
Dept of CSE
Program:- B.Sc in CSIT
Course title:- Digital Electronics and Pulse technique
Course code:- CSE 223

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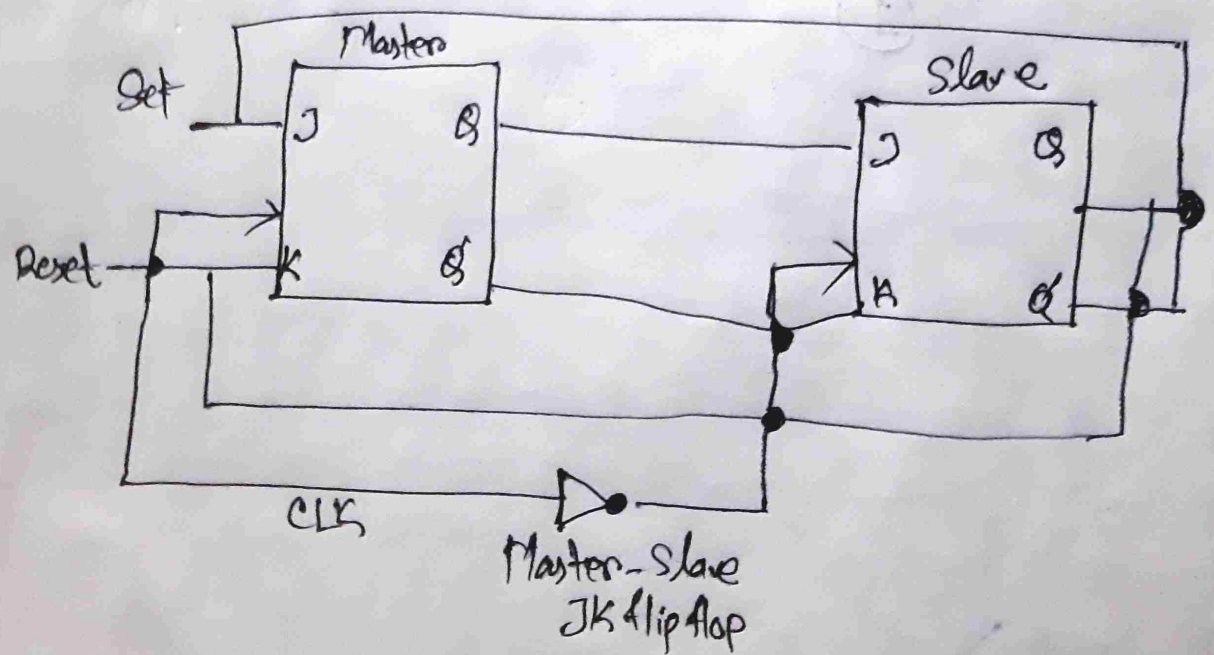
Final assesment

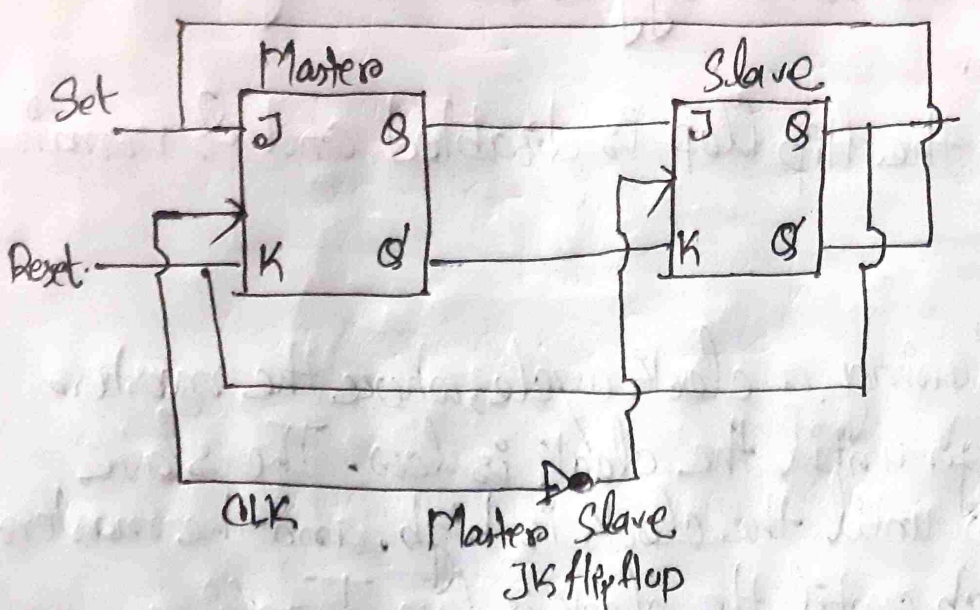
Ans to the Q no - 1(a)

Master-slave JK flip flop:-

The JK flip-flop faces a races round condition where the input becomes unstable if CLK is high for a long time. To avoid this, the Master-Slave JK flip flop is introduced. This is a combination of two JK flip flops connected in series, with one acting as the master and the other as the slave. The output from the master flip flop is connected to the ~~Q~~ slave flip flop's inputs, and an inverter is connected to the clock pulse.



Ans to the Q no - 1(b)



When the clock pulse goes to 1, the slave is isolated; J and K inputs may affect the state of the system. The slave flip flop is isolated until the CP goes to 0. When the cp goes back to 0 information is passed from the master flip-flop to the slave and output is obtained.

Firstly the master flip flop is positive level triggered and the slave flip flop is negative level triggered, so the master responds before the slave.

If J=0 and K=1, the high Q' output of the master goes to the K input of the slave and the clock forces the slave to reset, thus the slaves copies the masters.

If J=1 and K=0, the high Q output of the master goes to the J input of the slave and the negative transition of the clock sets

the slave copying master.

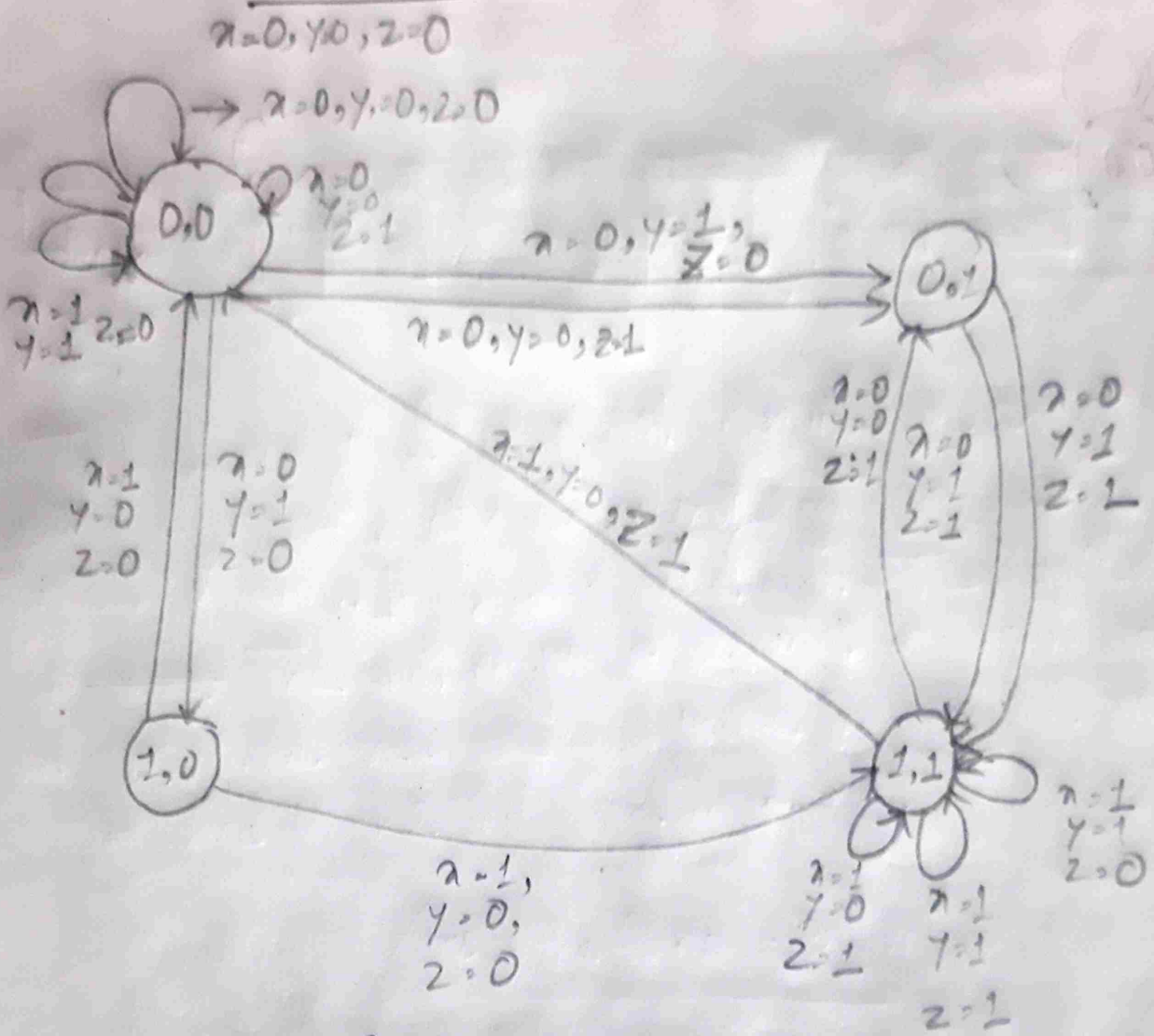
If J=1 and K=1, it toggles on the positive transition of the clock and thus the slave toggles on the negative transition of the clock.

If J=0 and K=0, the flip flop is disabled and Q remains unchanged.

Toggling occurs during a clock cycle, where the masters outputs remains high until the clock is low. The slave output remains low until the clock is high, and the masters output remains high until the clock is low. Toggling occurs once in a cycle.

This makes the Master-Slave JK flip flop a Synchronous device.

Ans to the Q no - 2(a)



x, y = input & z = output

		x, y	z
①	(0,0) → (0,0)	00	0
②	(0,0) → (0,1)	01	0
③	(1,0) → (0,0)	10	0
④	(0,0) → (0,0)	11	0
⑤	(0,0) → (0,1)	00	1

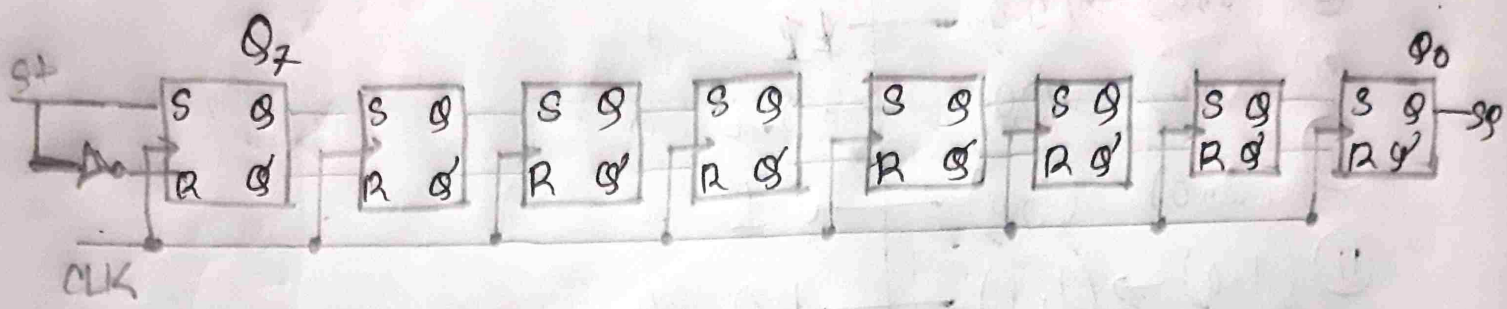
Present state ↙ new state ↙

		x	y	z
(6)	(0,1) → (1,1)	0	1	1
(7)	(1,1) → (0,0)	1	0	1
(8)	(0,0) → (0,0)	1	1	1
(9)	(0,0) → (0,0)	0	0	0
(10)	(0,0) → (1,0)	0	1	0
(11)	(1,0) → (1,1)	1	0	0
(12)	(1,1) → (1,1)	1	1	0
(13)	(1,1) → (0,1)	0	0	1
(14)	(0,1) → (1,1)	0	1	1
(15)	(1,1) → (1,1)	1	0	1
(16)	(1,1) → (1,0)	1	1	1

Present state

new state

Ans to the Q no- 3(a)



This is a digital integrated circuit that can send data parallely or serially converting and controlling output data in serial form. It is compatible with TTL logic devices.

The shift registers operates in two modes: parallel in serial out mode and serial in parallel out mode, controlled by the shift load input pin.

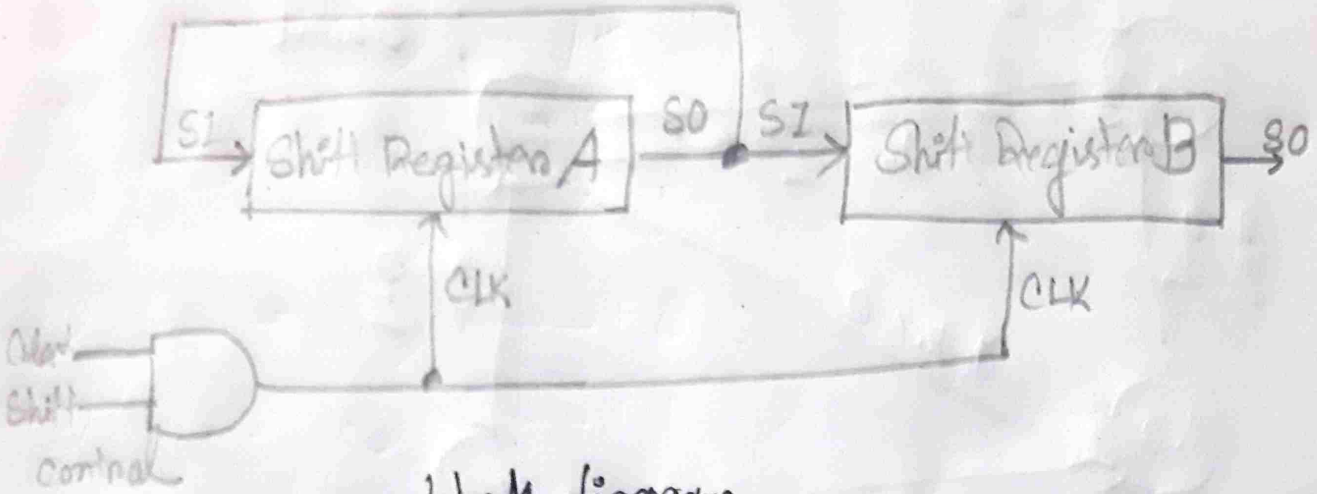
Ans to the Q no - 3(b)

① Serial mode - information is transferred and manipulated one bit at a time.

② Parallel mod - all the bits of the registers are transferred at the same time.

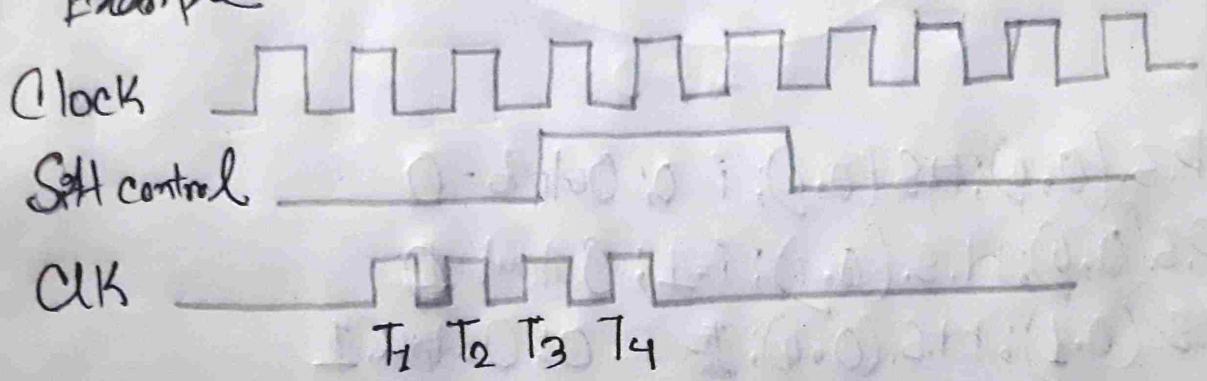
③ Shift control - determine when and how many times of the registers are shifted.

(iv) Register A is connected in circular mode in this circuit.



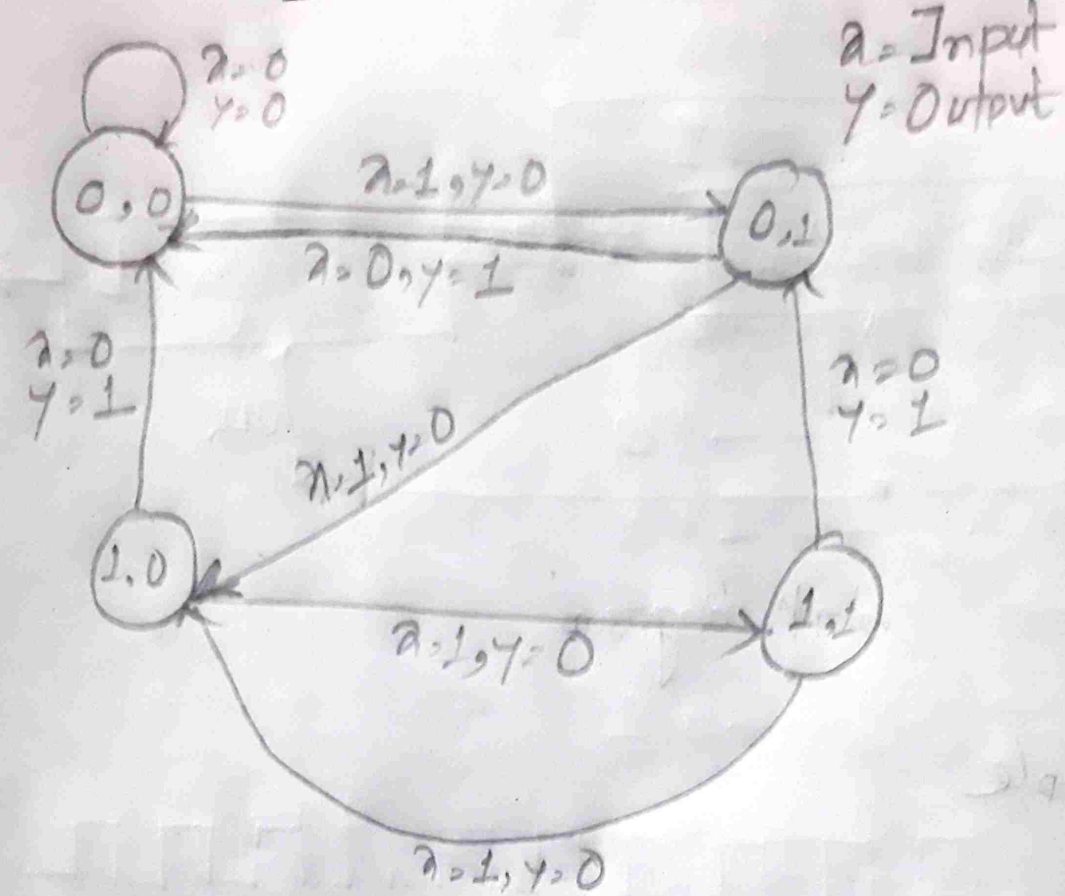
block diagram

Example



Timing pulse	Shift reg A	Shift reg B
Initial value	1 0 1 1	0 0 1 0
After T_1	1 1 0 1	1 0 0 1
After T_2	1 1 1 0	1 1 0 0
After T_3	0 1 1 1	0 1 1 0
After T_4	1 0 1 1	1 0 1 1

Ans to the Q no - 4(a)



① P.S. (0,0); N.S (0,0); i = 0; Output = 0

② P.S. (0,0); N.S. (0,1); i = 1; Output = 0

③ P.S. (0,1); N.S. (0,0); i = 0; Output 1

④ P.S. (0,1); N.S. (1,0); i = 1; Output = 0

⑤ P.S. (1,0); N.S. (0,0); i = 0; Output = 1

⑥ P.S. (1,0); N.S. (1,1); i = 1; Output = 0

⑦ P.S. (1,1); N.S. (0,1); i = 0; Output = 1

⑧ P.S. (1,1); N.S. (1,0); i = 1, Output = 0