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8th Batch (EV)
CSE

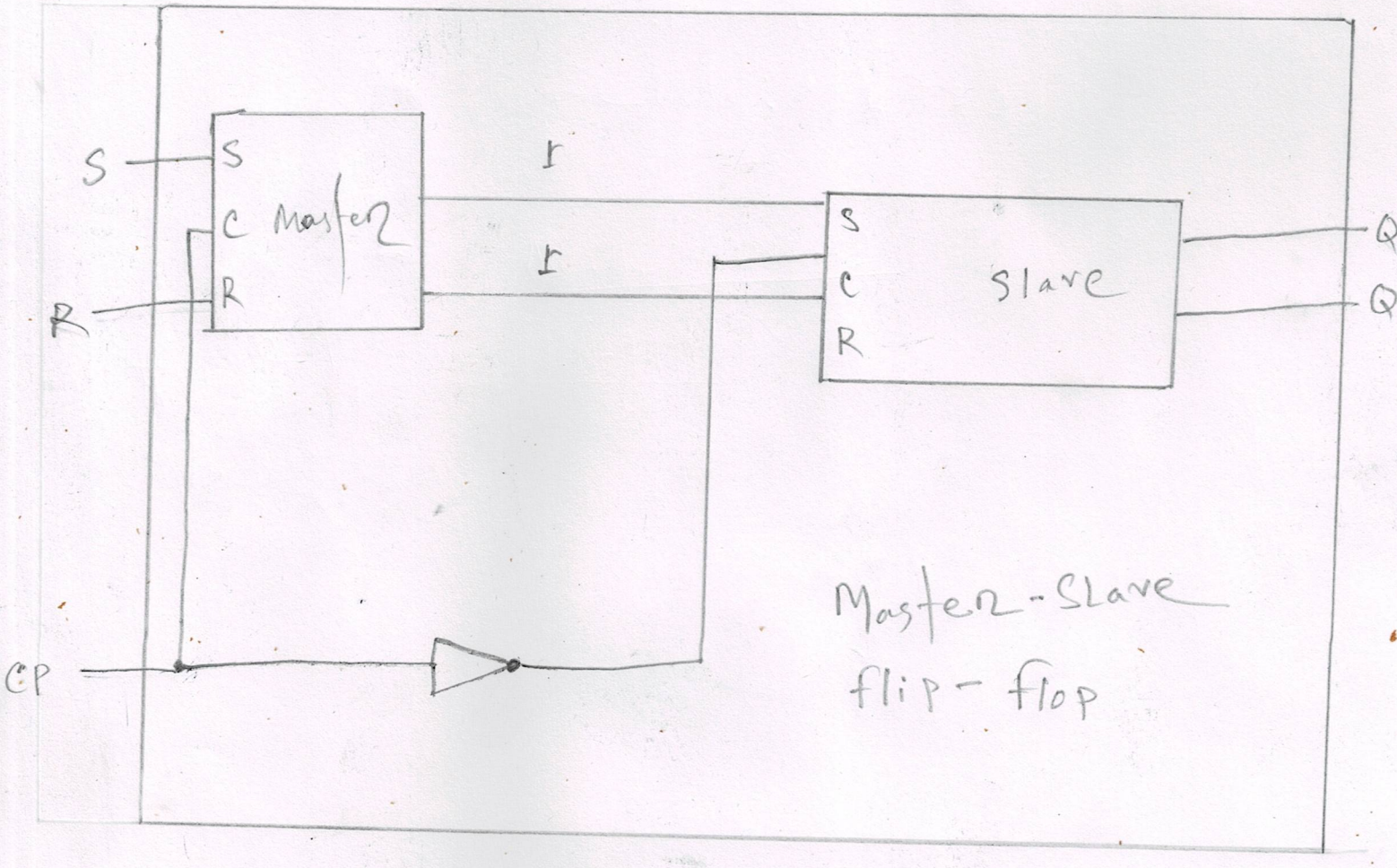
Course: Digital Electronic & Pulse Technique
Course code: CSE-223

Ans: the Q: NO: 01

(a) Master & Slave Flip-Flop:

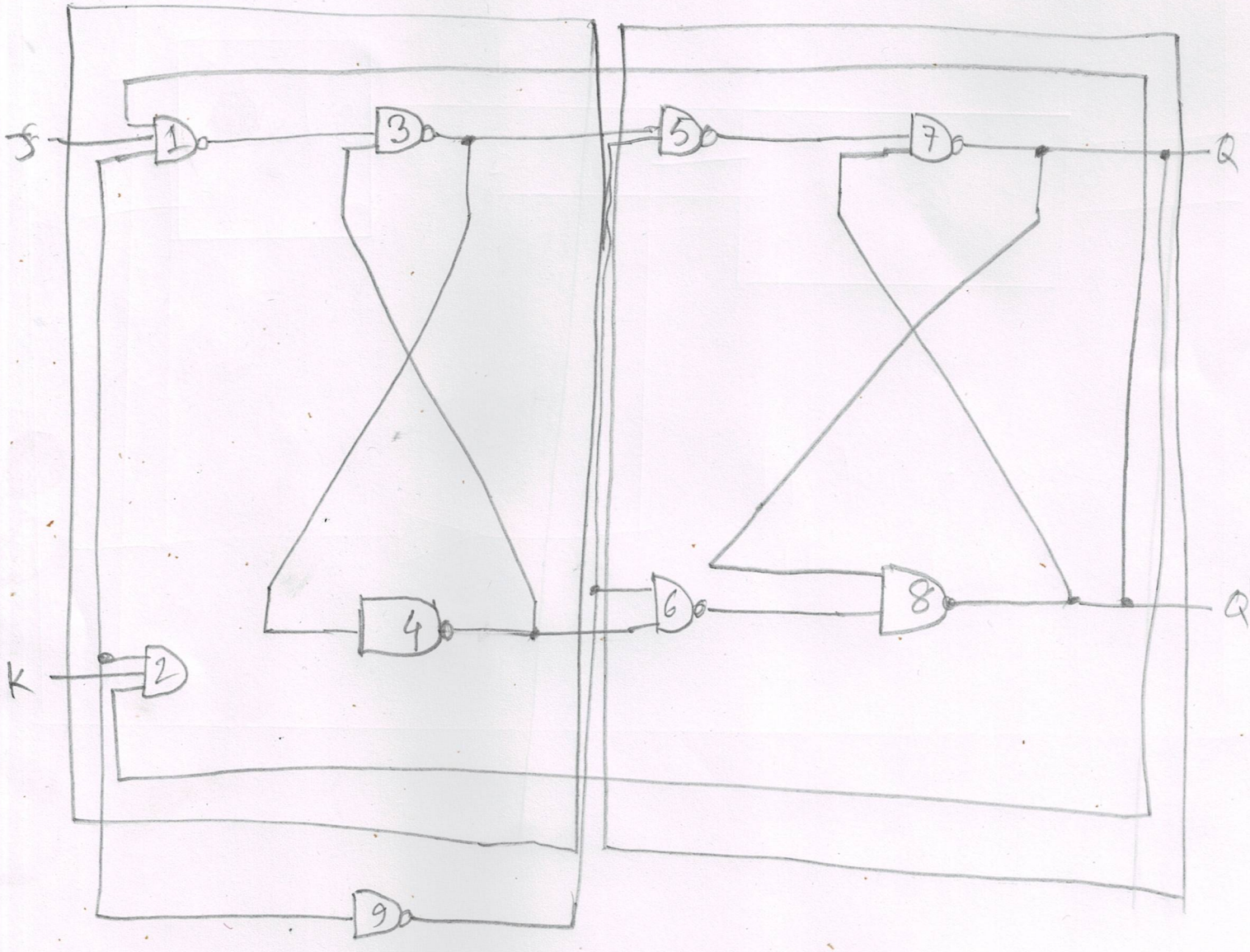
The concept samples the 2 input & always its output at the negative edge of the clock, CLK. When the clock in 0, the output of the inverter is 1. The slave latch is enabled & its output Q_s is equal to the master output 1. The master latch is disabled (CLK = 0) when the CLK changes to high, 0 input is transferred to the master latch. The slave remain disable as long as CLK is Low. ~~Any~~ change in the input changes Y, but not Q. The output of flip-flop can change when clk makes a transition $1 \rightarrow 0$

Master slave SR flip-flop (negative edge of triggered) are -


S
R
CP
S
C
R
Master
r
r
S
C
R
Slave
Q
Q
Master-Slave
flip-flop

Ans: the: q: no: 1 (b)

Master slave, flip-flop (negative, edge, triggered).



The circuit Samples the J input & changes it's Output at the negative edge of the clock cp

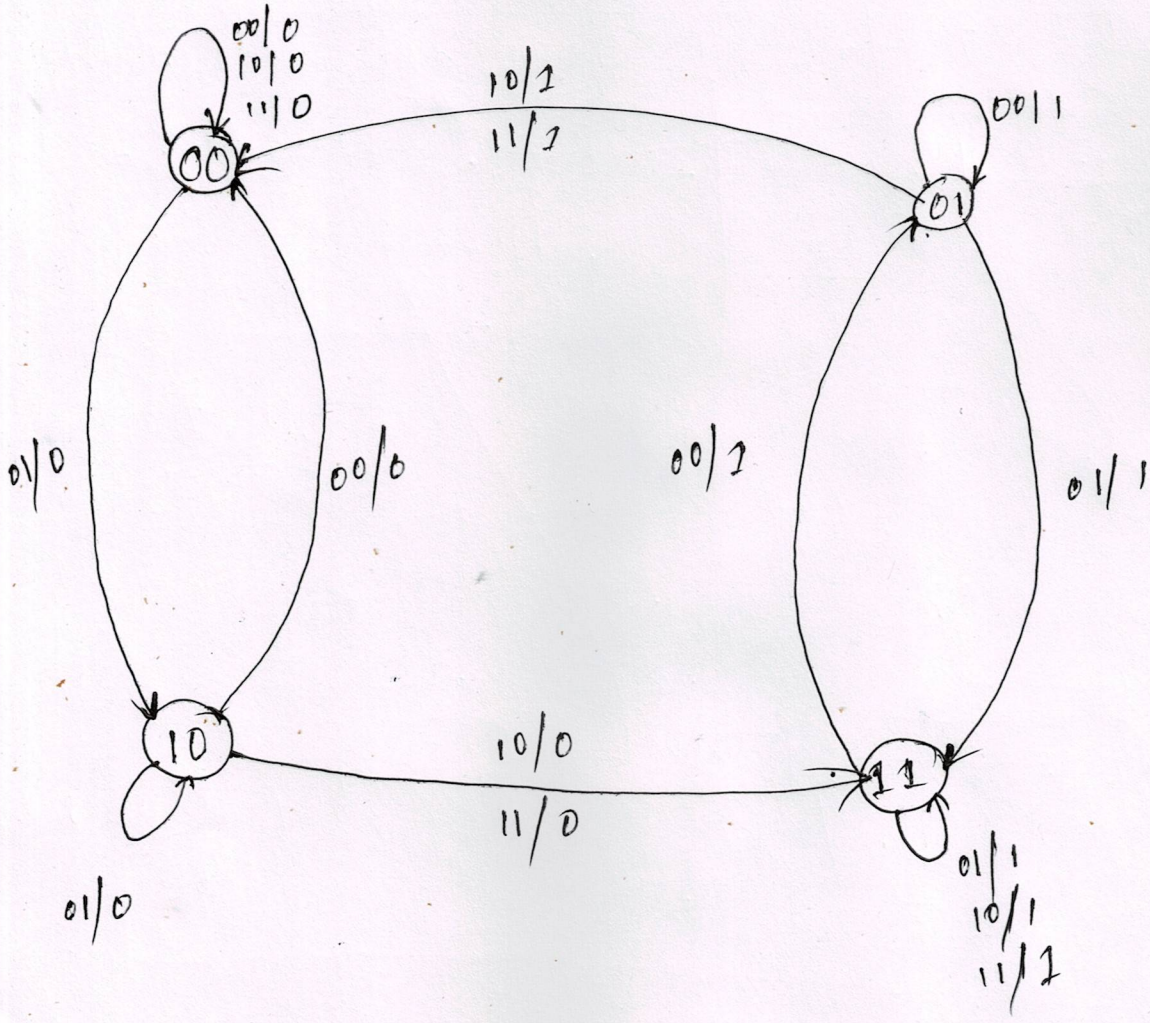
When the clock is 0, the output of the inverter is 1. The slave latch is enabled. AND Gate 6, 7, 8 is enabled. These gets which means slave's output is equal to the master output r. The master latch gate NO, 1, 2, 3, 4 is disable when ~~clk~~ (cp = 0).

when the cp changes to high, J input is transfer to the master latch. The slave remains disable as long as cp is low. Any change in the input changes r but not Q for J Input.

Similarly for K input circuit changes output for the negative edge of the clock, cp when the cp is 0, the output is 1. Then the slave latch is enable and its output r. for cp=0 the master latel is disable when cp is high the K input insent into master latch but when cp is low slave master disable. when cp is high the K input in sent into when changes the r is being changed for this but not Q'.

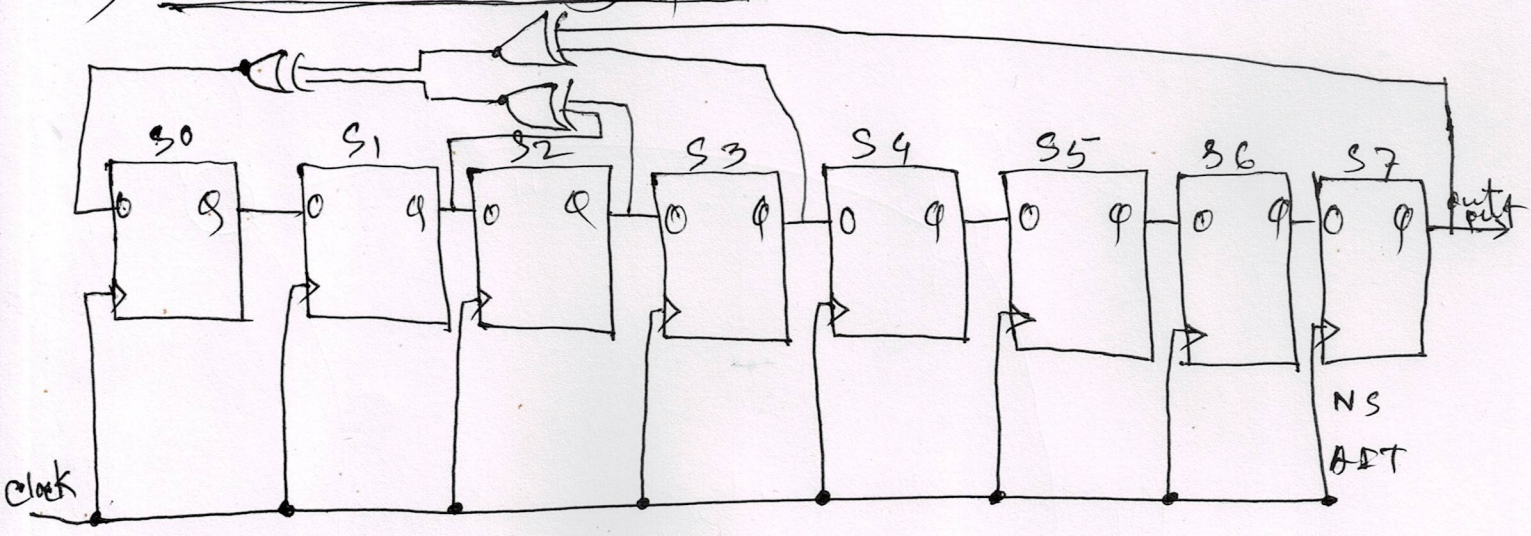
Ans: the q no 2

following state diagram is —



Ans: to the Q: NO: 3

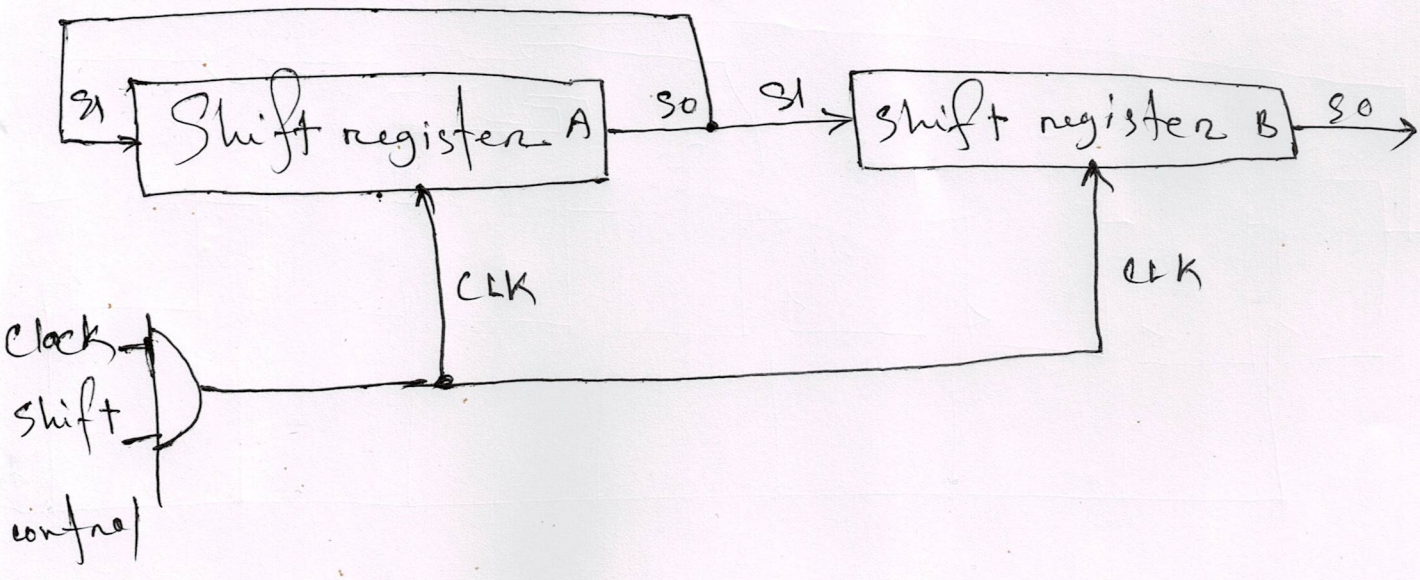
(a) 8-bit serial register:



The following register is a 8-bit serial register. There is clock for every cell. There is x-or gate for the register. Cell names are S0, S1, S2, S3, S4, S5, S6, S7. via a protocal which source to destination register for every cell there is input which is called D & Output is called Q. By combining all the functions the 8-bit serial register is built.

If the clock is disabled the registers turns to off mode there is x-or functions for the following gate.

(b) Serial transfer from register Reg A to Reg B

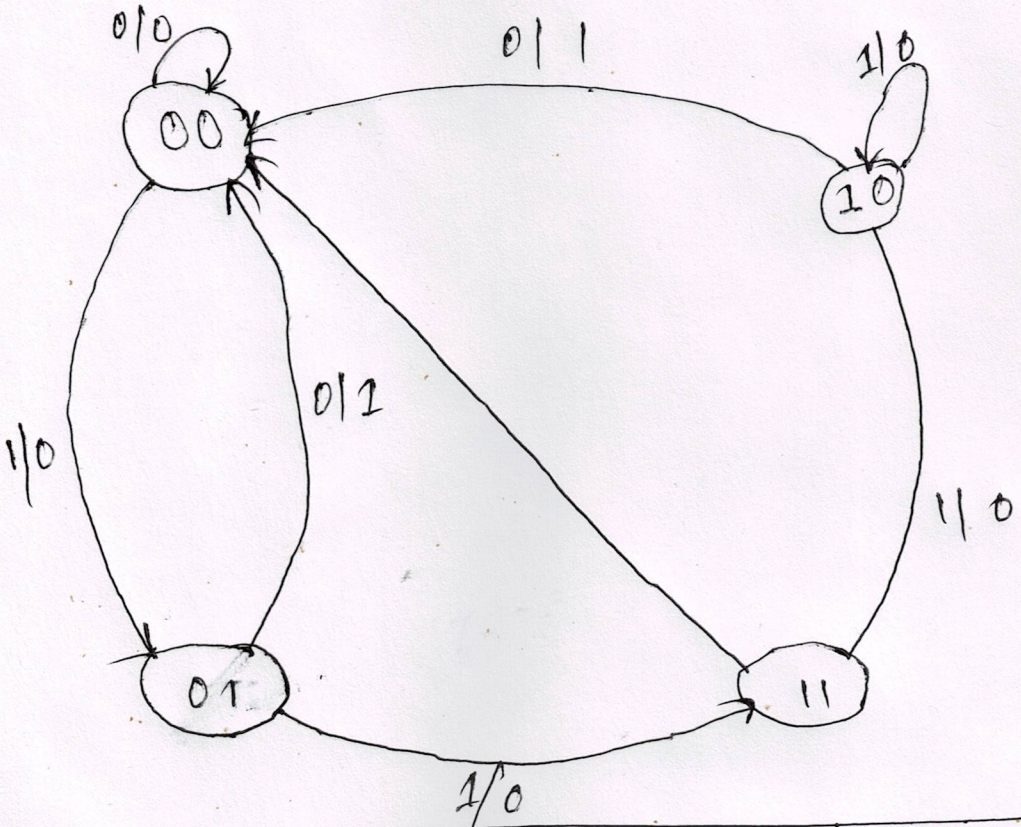


Sirial transfer example :—

Timing Pulse	Shift Register A	Shift register B
Initial Value	1011	0010
After T1	1101	1001
After T2	1110	1100
After T3	0111	0110
After T4	1011	1011

Ans: the Q: NO: 4

(a) state Diagram for the following question:-



Present state	Next state		output	
	x = 0	x = 1	x = 0	x = 1
A B	A B	A B	Y	Y
0 0	0 0	0 1	0	0
0 1	0 0	1 1	1	0
1 0	0 0	1 0	1	0
1 1	0 0	1 0	1	0

for the above transition table formulowure:-

$A(t+1) = Ax + Bx$

$B(t+1) = \bar{A}x$

$Y(t) = (A+B)\bar{x}$

for $x = 0$

$x = 1$