Name : Pardouse Lomat Jahan Rumpa

ID : 2219170041

Course Title : Digital Electronics and pulse technique

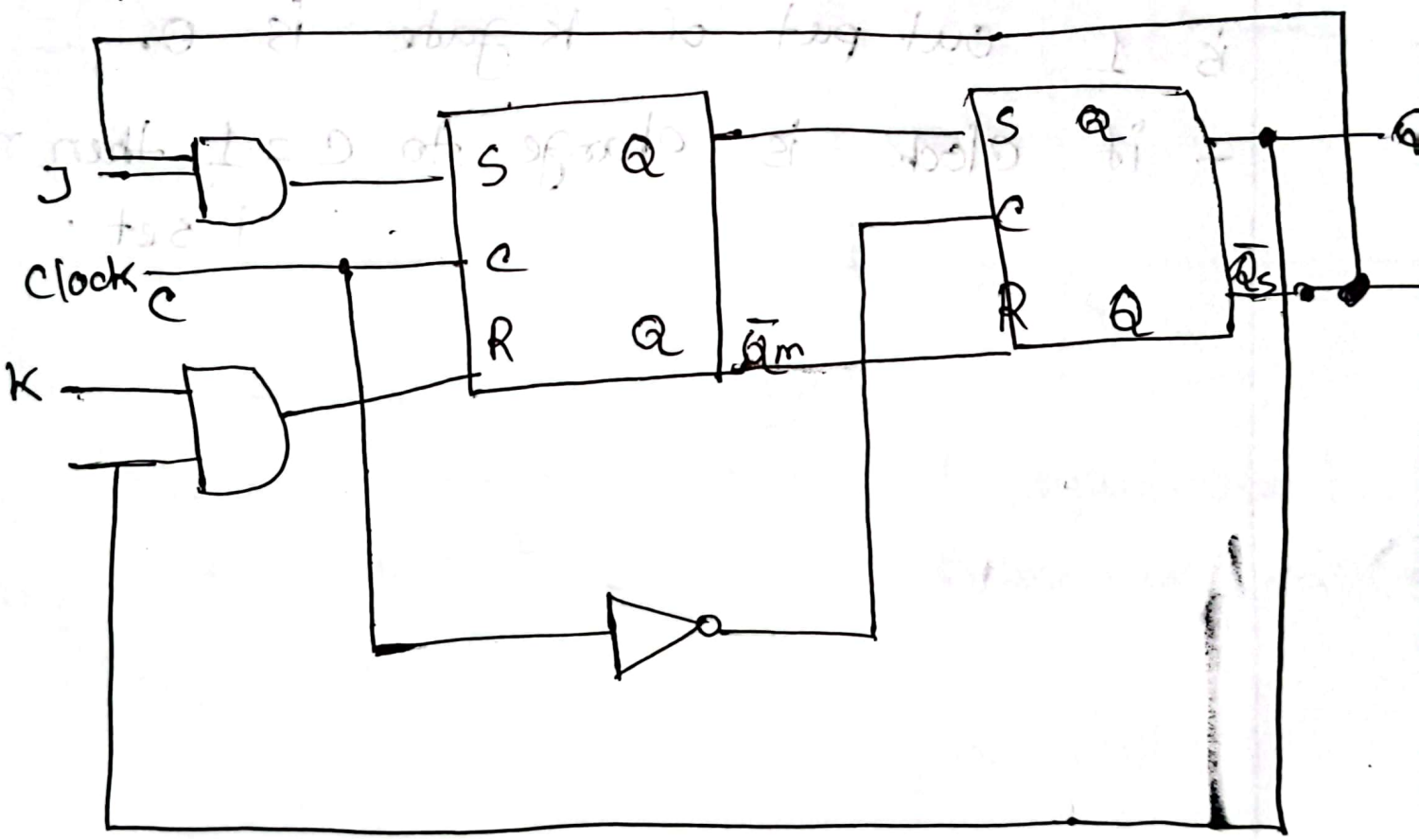
Course code : CSE-223

CSE - 22

Ans to the Ques. No - 01

(a) Ans Master & Slave flip-flop — A master slave flip-flope is made by connecting two JK flip-flops in a series configuration in which one acts as the master and another as a slave. ~~The~~

Example —



⇒ Assum in 1 - state, c=0, J=K=1.

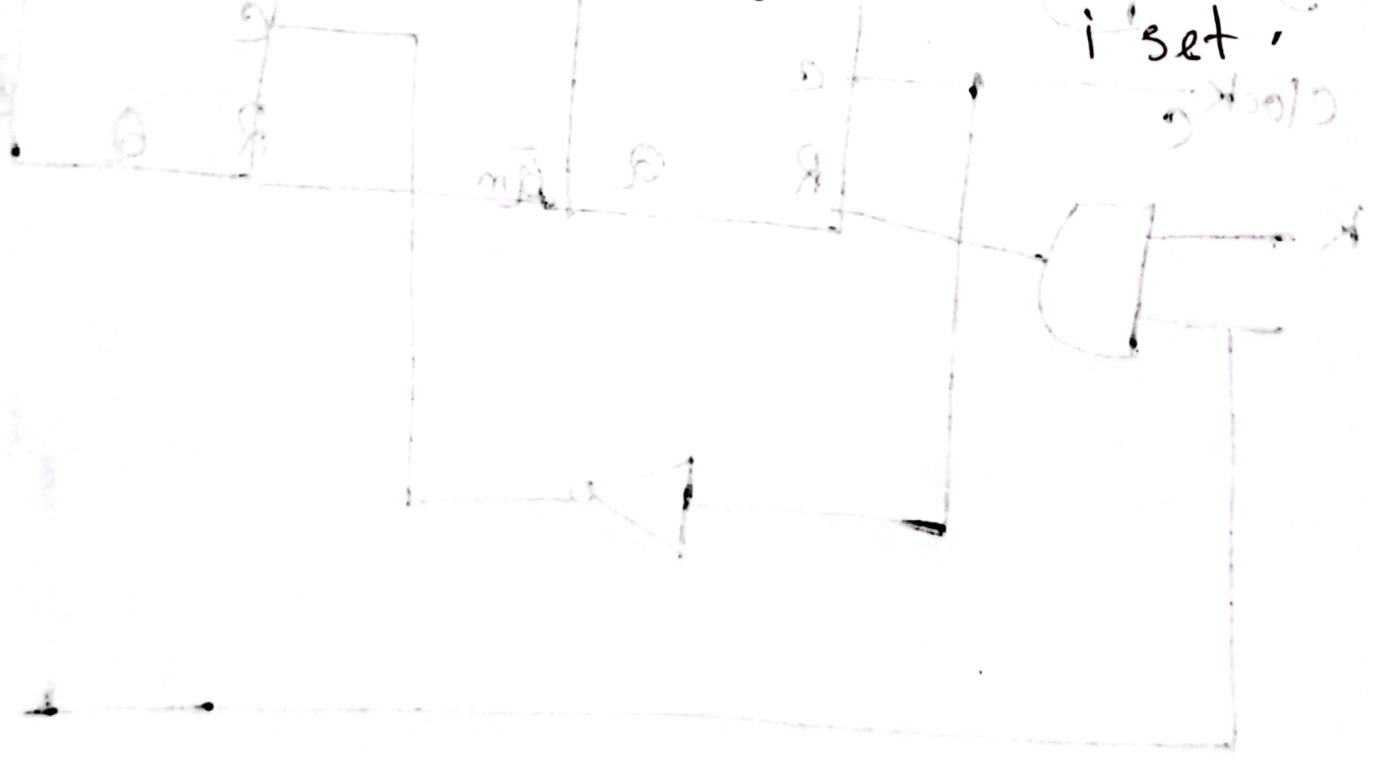
- Due to feedback, the Output of the J-gate is a Out put of K-gate is 1

- if clock is change to c=1 then master is reset.

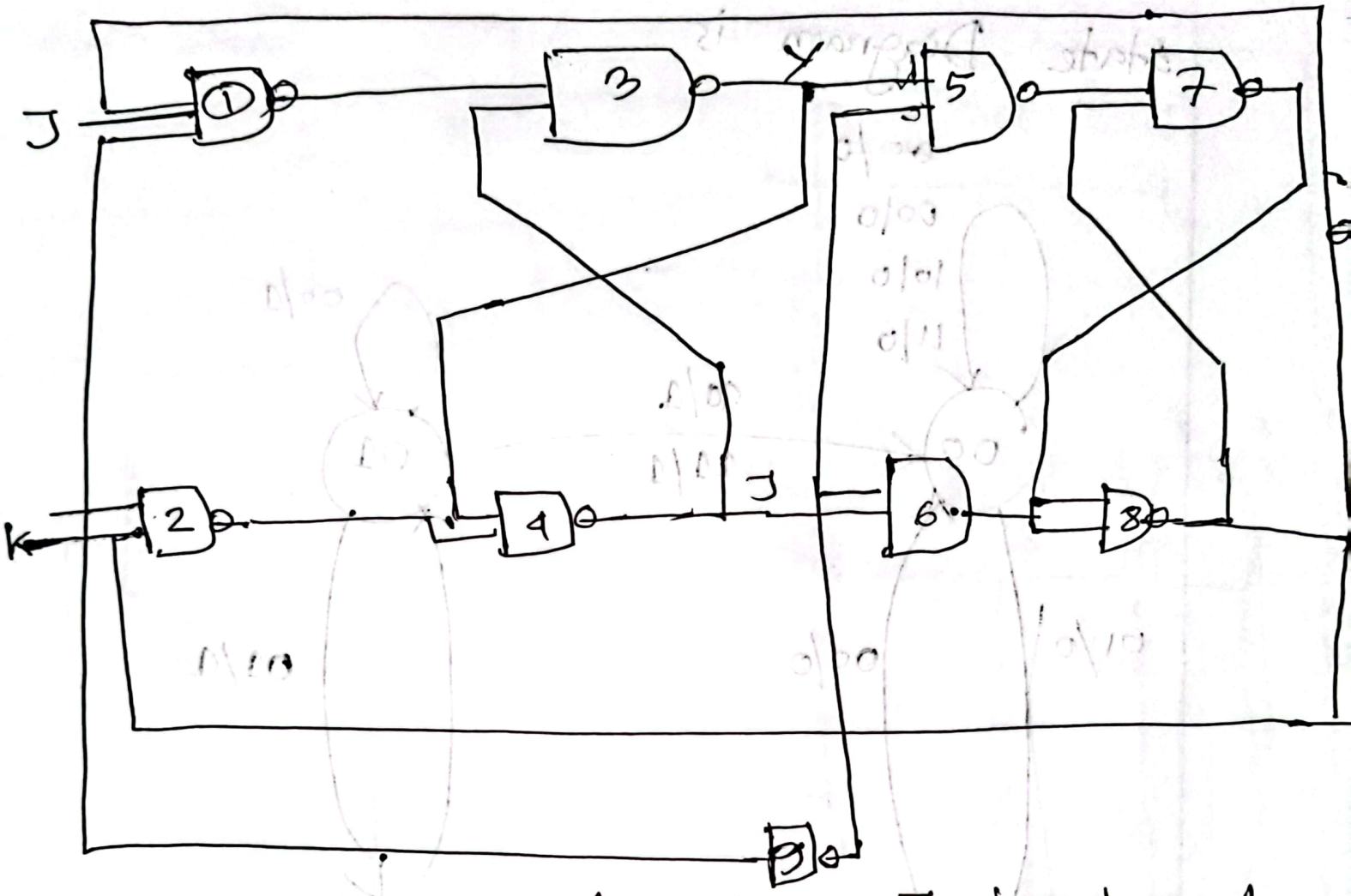
⇒ Assum in 0 - state, c=0, J=K=1

- Due to feedback, the Out put of the J-gate is 1 out put of K gate is 0.

- if clock is change to c=1, then master is set.



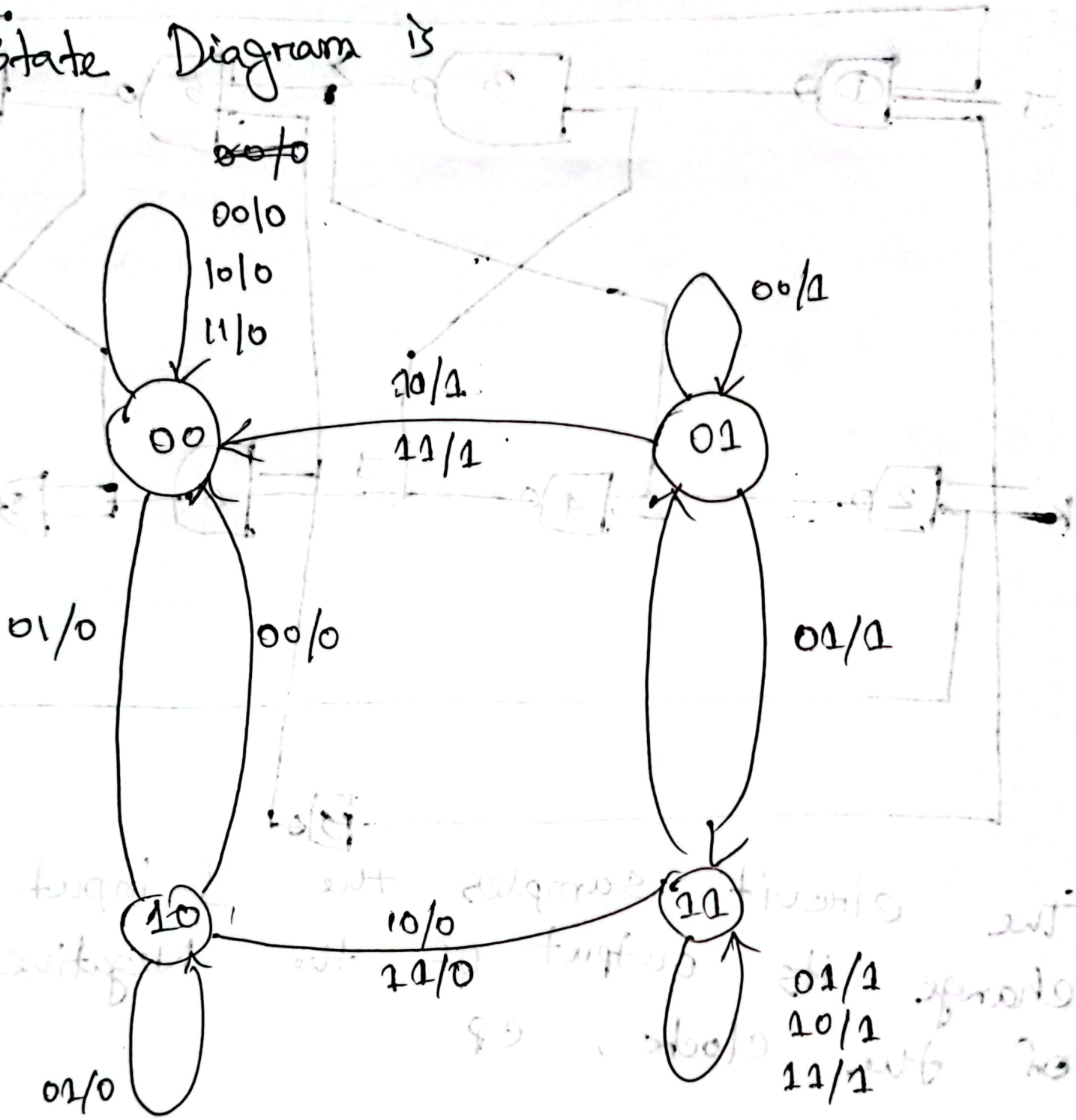
① (b) Master-Slave Flip-Flop using JK = FF



the circuit samples the J, input and change its output of the Negative edge of the clock, CP

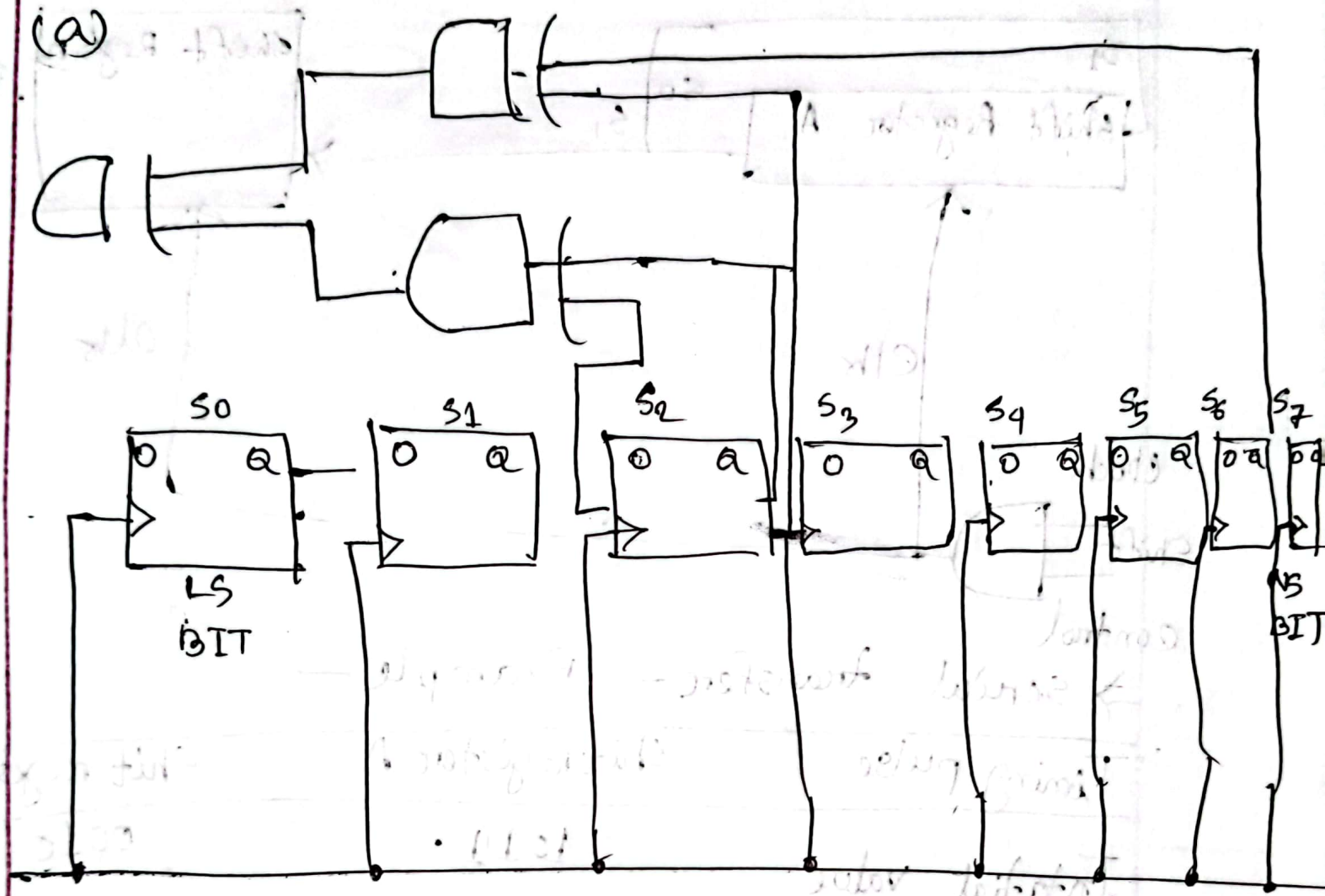
Ans : to the Ques No-2(a)

State Diagram is

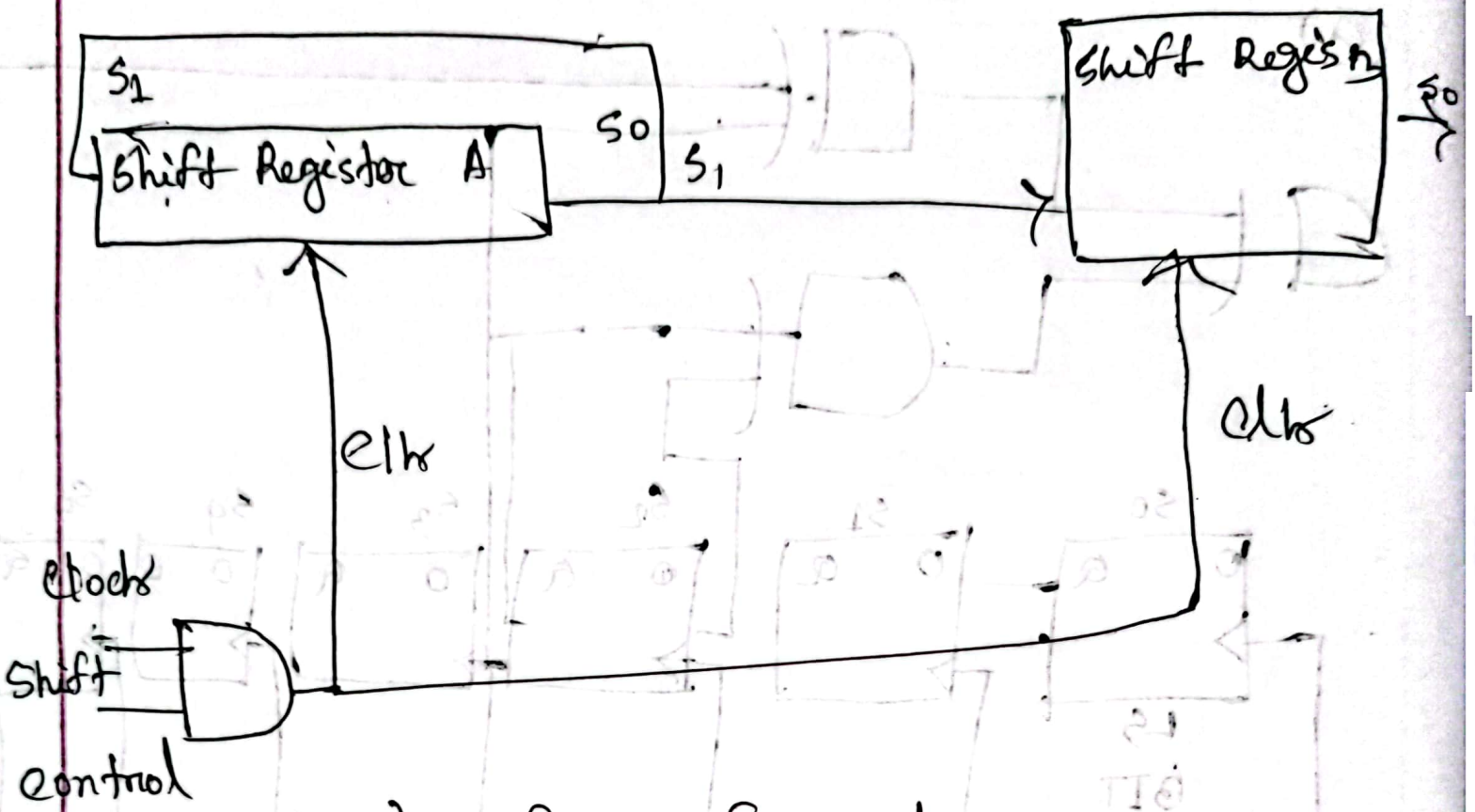


Ans to the Ques. No - 3

(a)



(b)



⇒ Serial transfer — Example —

Timing pulse	Shift Register A	Shift register
Intatial value	1011	0010
After P_1	1101	1001
After P_2	1110	1100
After P_3	0111	0110
After P_4	1011	1011