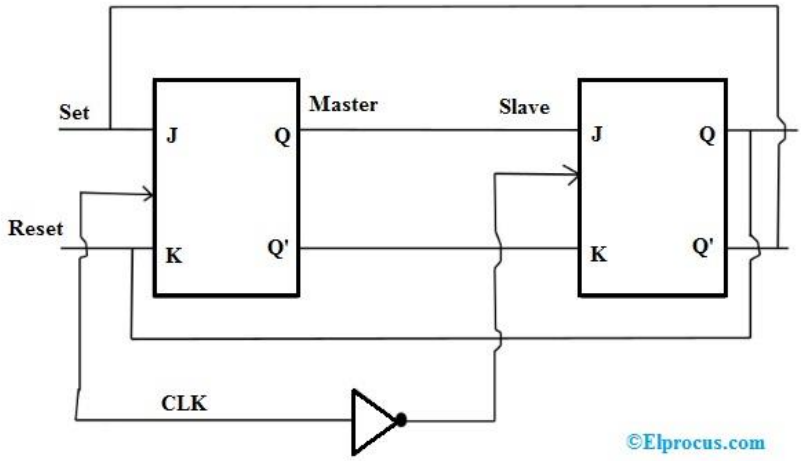
Victoria University of Bangladesh
Name: Md. Ziaul Hoque "Sohel"
Student ID: 2221220031
Course Title: Digital Electronics and Pulse Technique
Course Code: CSE-223
Batch: 22nd (evening)
Semester: Fall-2023

Ans to the Que No 1(A)

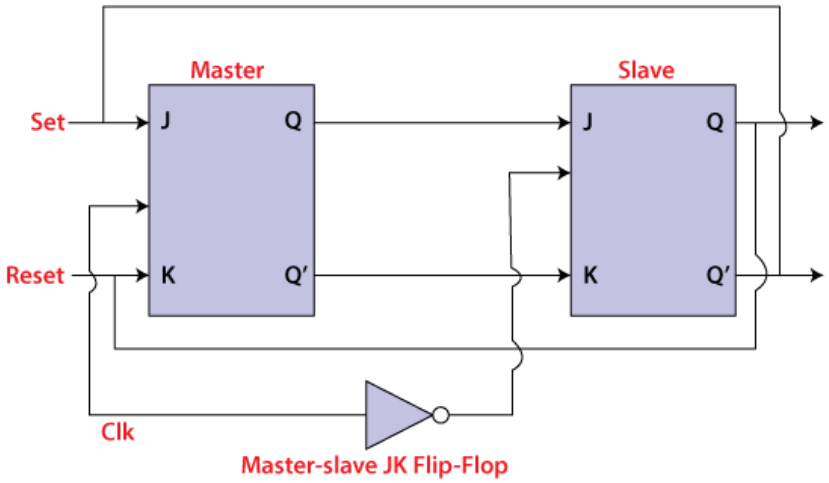
Master-Slave flip flop:

Basically, this type of flip flop can be designed with two JK FFs by connecting in series. One of these FFs, one FF works as the master as well as other FF works as a slave. The connection of these FFs can be done like this, the master FF output can be connected to the inputs of the slave FF. Here slave FF's outputs can be connected to the inputs of the master FF.
In this type of FF, an inverter is also used addition to two FFs. The inverter connection can be done in such a way that where the inverted CLK pulse can be connected to the slave FF. In other terms, if CLK pulse is 0 for a master FF, then CLK pulse will be 1 for a slave FF. Similarly, when CLK pulse is 1 for master FF, then CLK pulse will be 0 for slave FF.



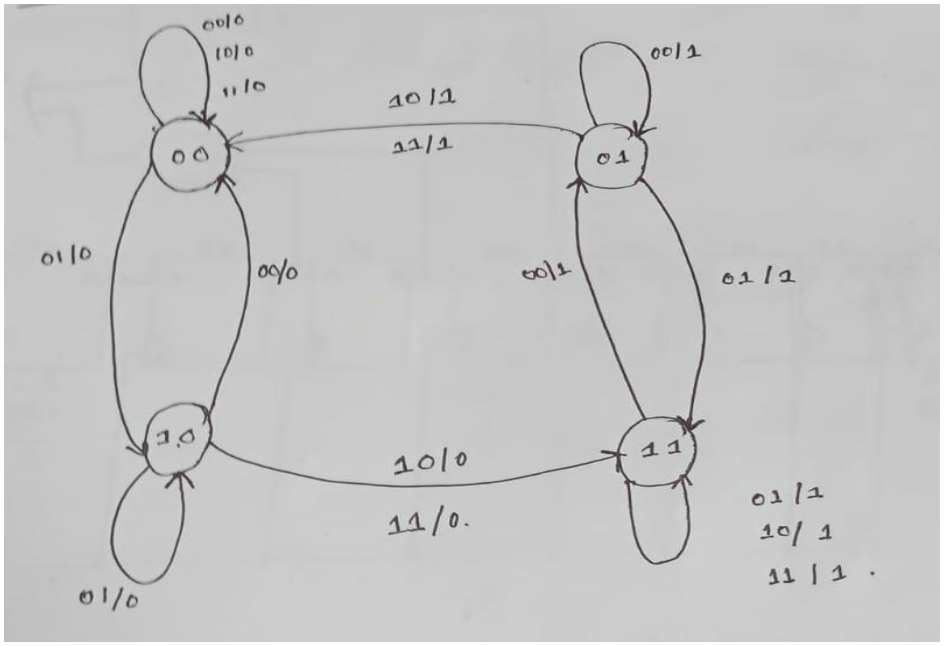
Ans to the Que No 1(B)

The master-slave flip flop is constructed by combining two JK flip flops. These flip flops are connected in a series configuration. In these two flip flops, the 1st flip flop work as "master", called the master flip flop, and the 2nd work as a "slave", called slave flip flop. The master-slave flip flop is designed in such a way that the output of the "master" flip flop is passed to both the inputs of the "slave" flip flop. The output of the "slave" flip flop is passed to inputs of the master flip flop.
In "master-slave flip flop", apart from these two flip flops, an inverter or NOT gate is also used. For passing the inverted clock pulse to the "slave" flip flop, the inverter is connected to the clock's pulse. In simple words, when CP set to false for "master", then CP is set to true for "slave", and when CP set to true for "master", then CP is set to false for "slave".

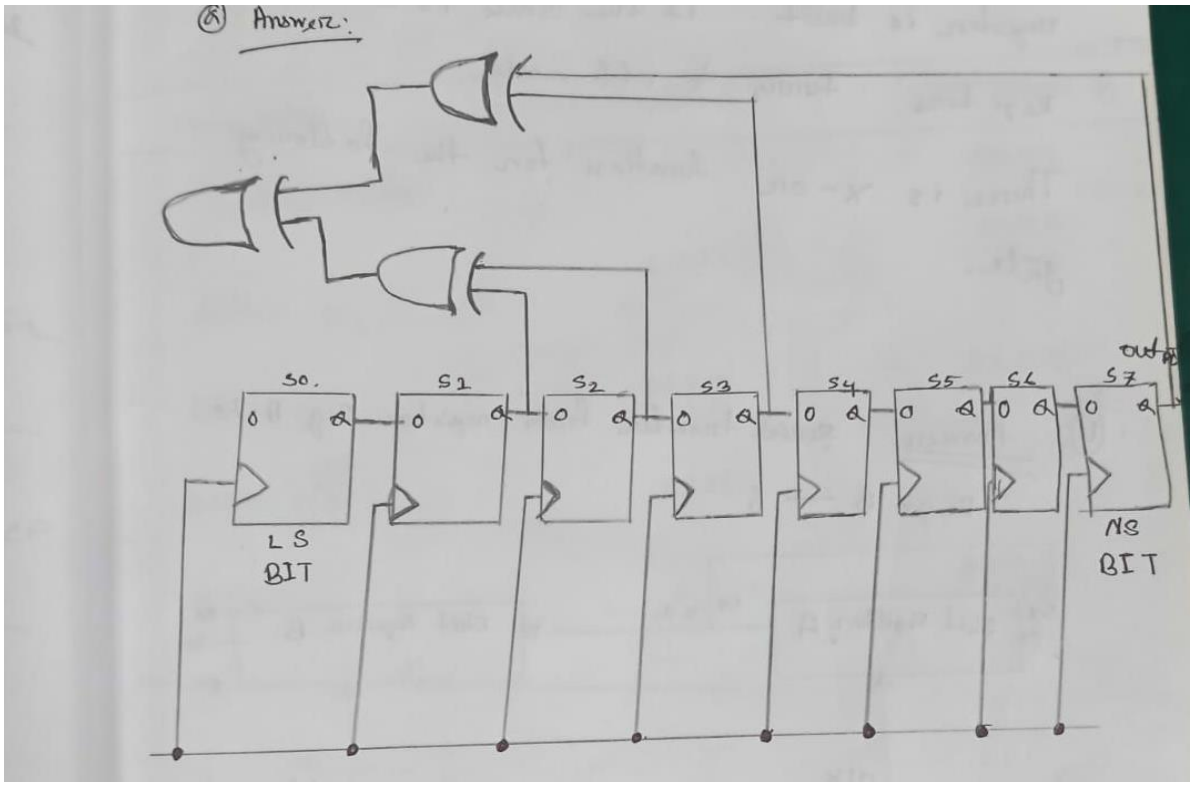


Ans to the Que No 2 (A)

State Diagram:



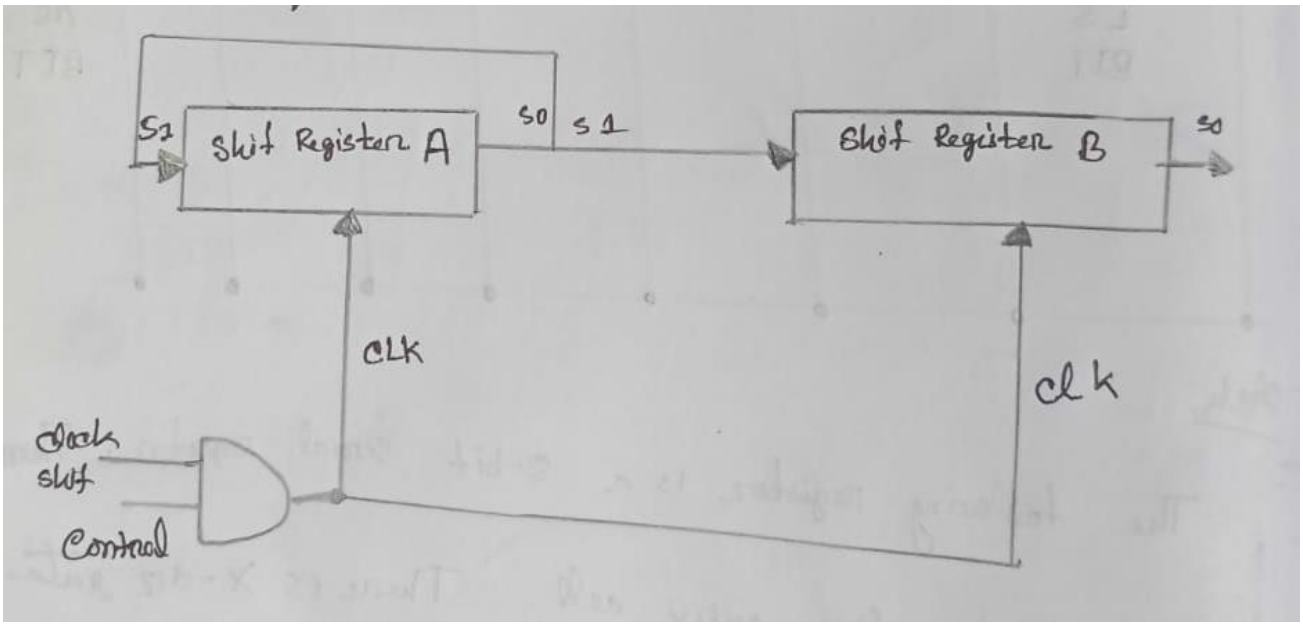
Ans to the Que No 3 (A)



Clock: The following registrar is a 8 bit serial register. There is clock for every cell & X-OR Gate for the register cell names are S0,S1……S7. All the cell ml connected via a protocol which source to destination register for enemy cell there is input which is called O and output is called Q. By combining all the functions the 8-bit Serial register is built. If the clock disabled the resisters turns to off mode. There is X-OR function for the following gate.

Ans to the Que No 3 (B)

Serial transfer from register A to Replace B

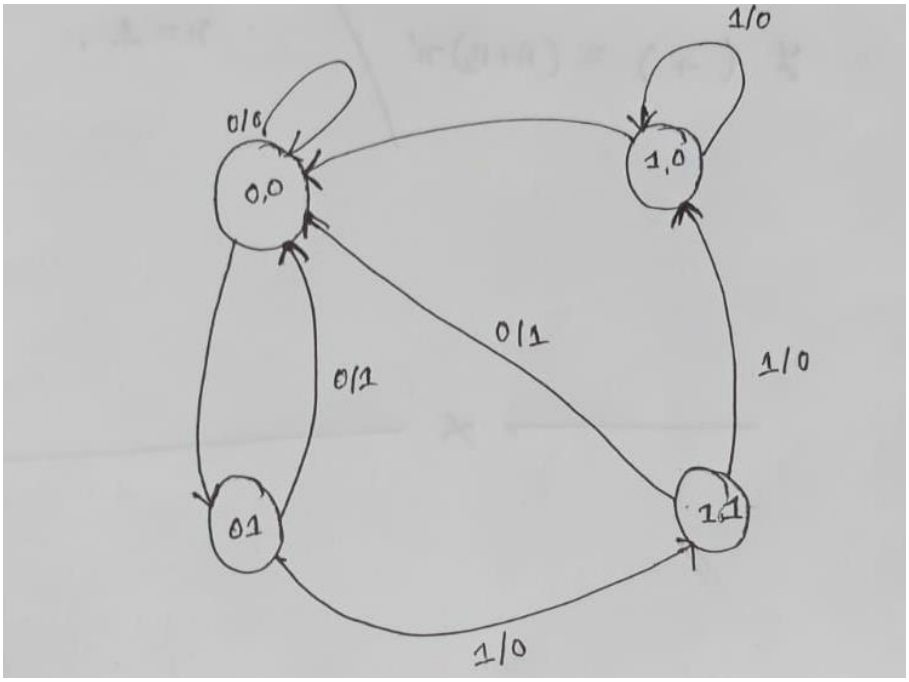


Serial Transformer Example:

Training Plus	Shift Register A	Shift Register B
Intuited B value	1011	0010
After P1	1101	1001
After P2	1110	1100
After P3	0111	0110
After P4	1011	1011

Ans to the Que No 4

Diagram for the given Table:



Present State		Vet State		Output	
		X = 0	X = 1	X= (1)	X=1
A	B	A B	A B	Y	Y
0	0	0 0	0 1	0	0
0	1	0 0	1 1	1	0
1	0	0 0	1 0	1	0
1	1	0 0	1 0	1	0

For the avobe transtition table for mulis one

A (+ + 1) = Ax + Bx	for x = 0, x = 1
B (+ + 1) = A' x	
Y (+) = (A + B)x'	

- END -