Victoria University
of Bangladesh

Final Assessment

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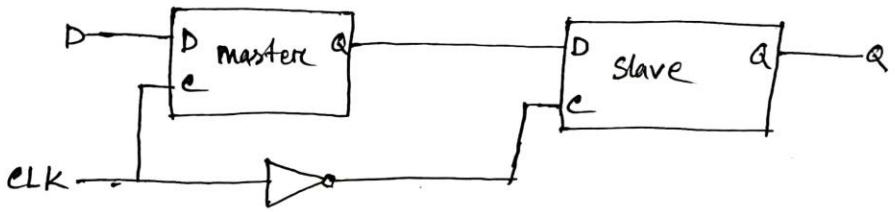
Answer to the question No 1(a)

1.a) Answer:- master slave Flip flop is a type of clocked flip-flop consisting of master and slave elements that are clocked on complementary transfetion of the clock signal.

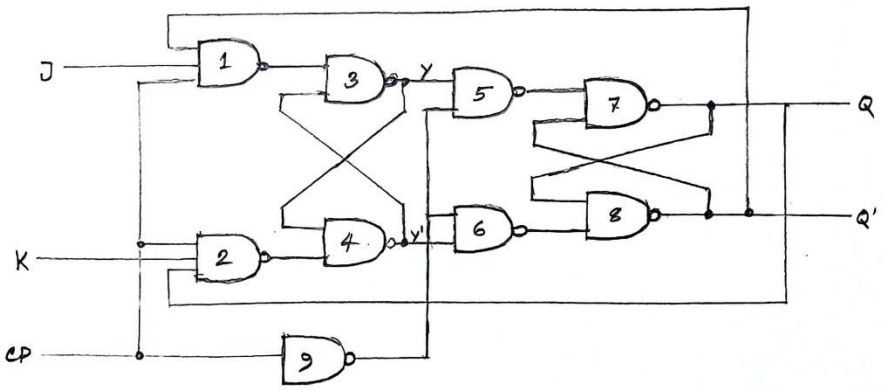


master-slave Flip Flops.

- The circuits sample the D input and changes its output at the negative edge of the clock, CLK.
- when the clock is 0, the output of the interter is 1. the slave latch is enabled and its output Q is equal to the master output y. the master latch is disabled (CLK=0)
- when the CLK changes to high D input is transferred to the master latch: the slave remains disable as long as CLK is low. any change in the input changes y. But not Q.
- the output of the flip-flop can change when CLK makes a transition $1 \rightarrow 0$.

Answer to the question no 1(b)

1.b) Draw master and describe the master-slave FLIP-FLOP using JK



describe:-

* TWO JK-FLIP-FLOPS: labeled "master" and "slave" in the top-right corner
* clock signal (CP): Represented by a square wave symble on the left.
* inverted clock signal (CP): created by the inverter(not Gate) below the clock signal and connected to the slave flip flop
* J & K inputs: shared by both flip-flops, controlling their next state.
* Qm and Qs outputs:- outputs of the master and slave FLIP flops.

Functionality:- master operation during positive clock edge (CP High)

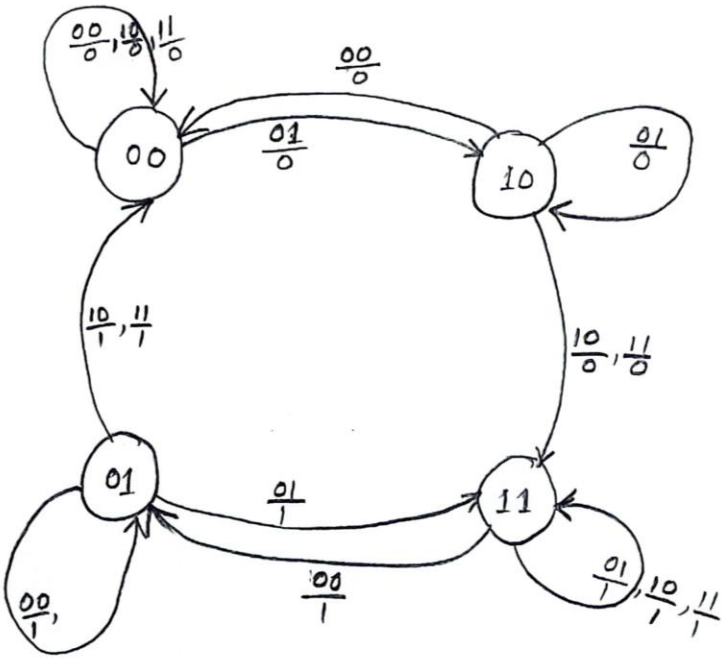
- J and K inputs determine the next state of the master flip flop.
- slave FLIP-FLOP is isolated

Slave operation during negative clock edge (CP Low)

- master FLIP FLOP output becomes the new data for the slave flip-flop
- slave flip-flop captures this data, updating its Q_S output
- master flip flop is isolated (CP High)

Answer to the question NO 2(a)

2a) Answer:- Draw the state diagram for the given table.

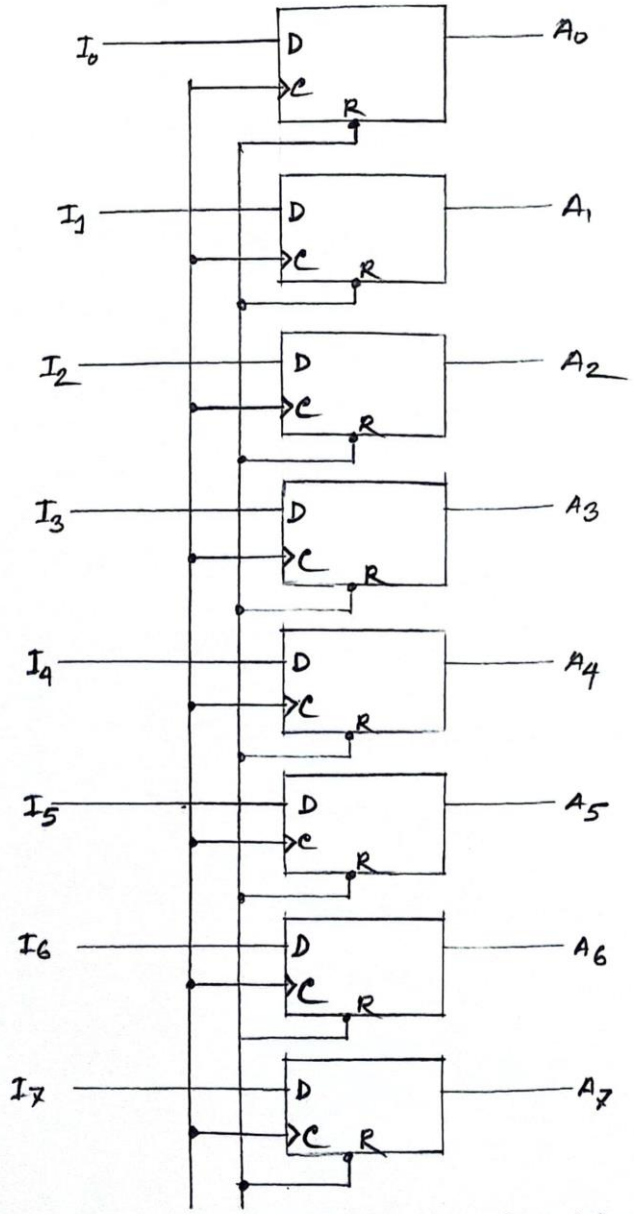


output depends on state

Next state depends on input and current state

Answer to the question no 3(a)

3.a) Answer:- An 8 bit serial register is a type of data storage element that stores binary information in a sequential manner. It is often used in digital system for tasks such as data transmission, shift operation, temporary store data.



Eight Bit serial register

① Flip-Flop (D_0-D_7): each rectangle represent a flip flop, which is a binary storage element capable of storing one bit of data. in this case. there are eight flip flops labeled D_0 through D_7 collectively forming an 8 bit register.

② serial-Data flow:- the arrows indicate the flow of data in a serial manner. data is shifted from one flip-flop to the next sequentially. this means that each clock cycle-or shift operation.

③ shift register operation:- the serial register is often used as a sift register. serial data is loded into the first flip-flop (D_0) and subsequent clock pulse shift the data to the right.

④ clock input:- The shift of data from one flip-flop to the next is controlled by a clock signal. each rising or falling edge of the clock triggers the shift operation.

⑤ parallel output:- although the data is shifted serially. the parallel outputs (A_0 to A_7) can be used to read the entired content of the register simultaneously.

Answere to the question NO 3(b)

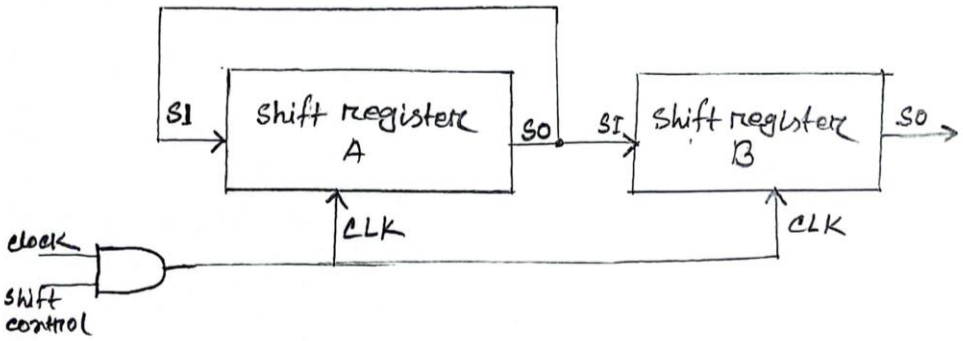
3.b. Answer:- There are two main ways to achieve sorcial transfer frurom register A to B.

① using a shift register:- this method involves connecting the serial output (SO) of register A to the serial input (SI) of a shift register. then connect the clock signal of both register together. with each clock pulse, the data from A will be shifted into the first bit of the shift register and simultaneously all other bits within the shift register will move one position to the right. after N clock pulse the entire data from A will be present in the shift register and finally connecting the SO of the shift register to the SI of register B and providing another N clock pulse will transfer the data from the shift register to register B.

② using dedicated controllers:- this method is more complex but offeres greater flexibility. you can use a microcontroller or any programmable logic device to control the transfer process. The controller can read data from register A one bit at a time and then write it to register B. shift the existing data within B one position to the right each data write

Here some additional consideration for the serial transfer.

- clock synchronization.
- Data format.
- Error detection/correction.
- Hardware resources.



Answer to the question no 4(a)

4.a) Draw the state diagram for the table

state table

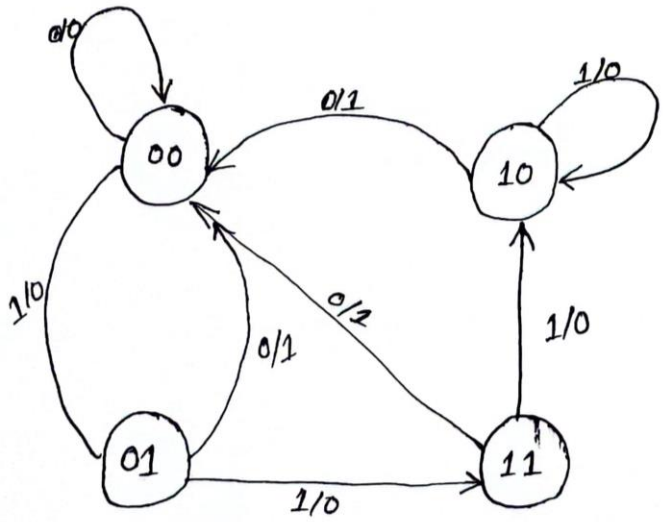
$A(t+1) = Ax + Bx$

$B(t+1) = A'x$

$Y = (A+B)x'$

present state		next state		output	
		x=0	x=1	x=0	x=1
A	B	A	B	Y	Y
0	0	0	0	0	0
0	1	0	1	1	0
1	0	0	1	1	0
1	1	0	1	1	0

state diagram



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