Victoria University of Bangladesh

Department of Computer Science & Engineering

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Final Assessment

Program: B.Sc in (CSE)

Semester: Fall-2023

Batch: 22nd (Evening)

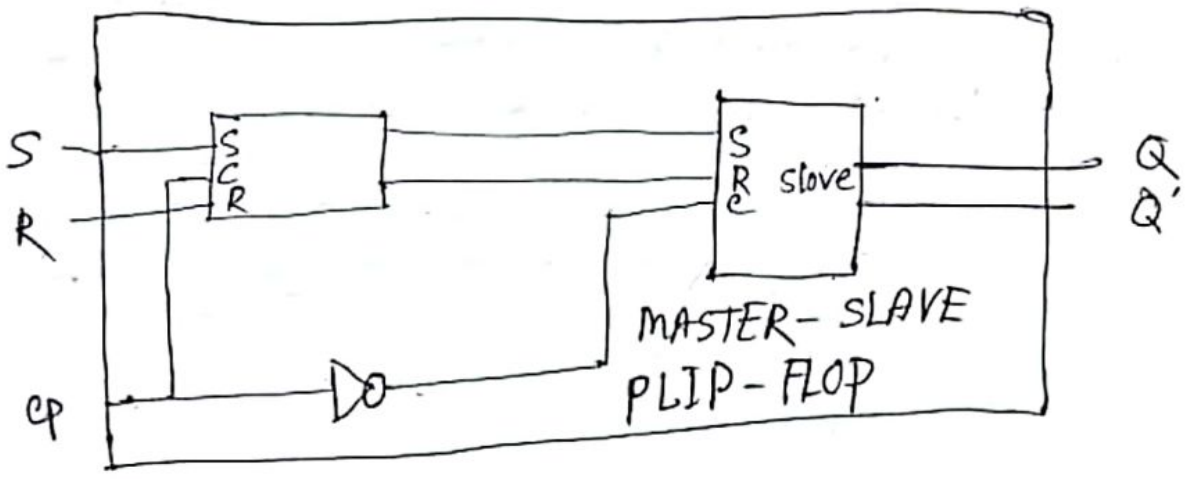
Course code: CSE-223

Course Title: Digital Electronics and pulse Technique.

## Ans to the Ques No-1(a)

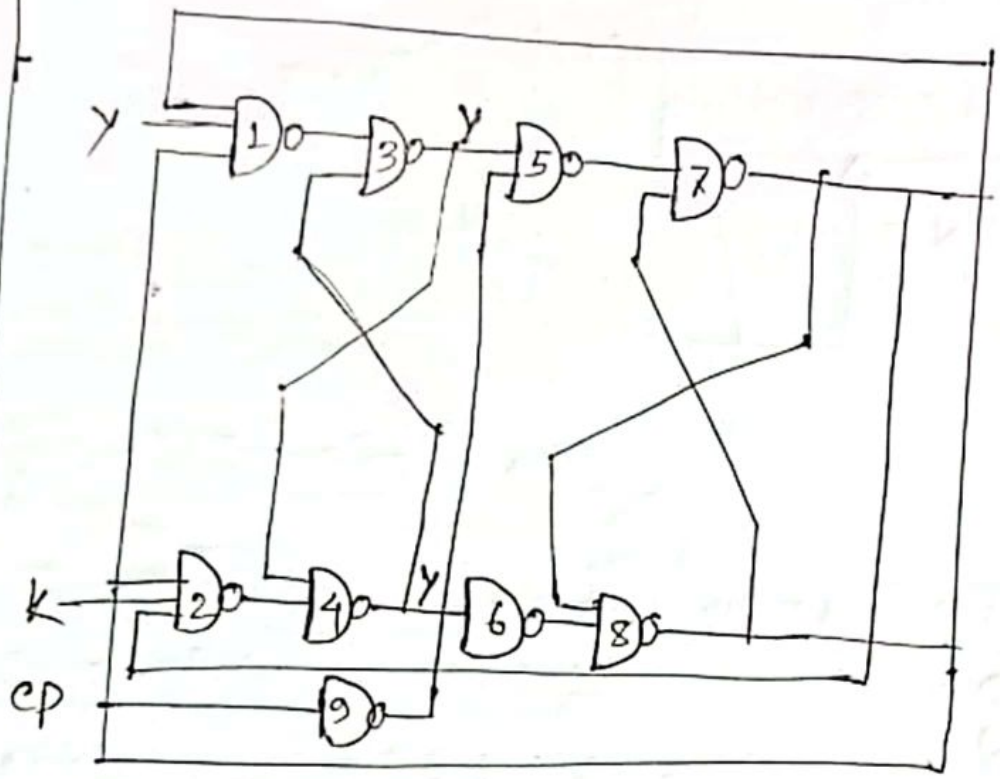
## MASTER & SLAVE PLIP. PLOPS

The circuit Samples the D input and changed its output at the negative edge of the clock at the negative edge of the clock, clk. When the clock in 0, the out-put of the inverter is it. The Slove later is erobled and its output Q is eqed to the master output @ y. The master later is disabled (CLK=0) when the CLK changes to nigh. D input is transforied to the master. Latch the Solve remains disabled as lord as clk is low. Any change is the input changs y, but not Q. The output of the flip flop can change when clk makes a transition 1 → 0. ☐ Master slave SR flip-flop (negative edge triggered)



Ans to the ques No-1 (b)

MASTER Slave JK flip-flop (Negative edge triggered)—

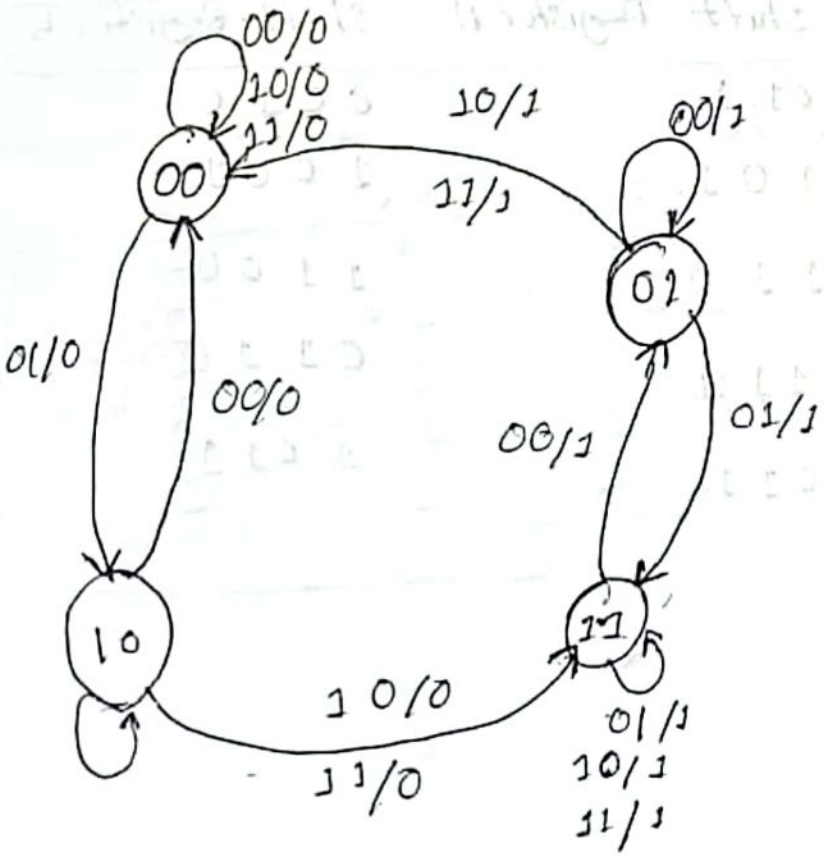



The circuit samples the J input and changes its output of the negative edge of the clock, cp. when the clock is 0, the output of the inverter is 1. The slave latch is enabled AND gate 5, 6, 7, 8 is enabled. These yields which means slave is output y. The master latch gate No 1, 2, 3, 4 is disable latch (cp=0). when the cp changes to high, J input is transferred to the master latch. The slave remains disabled as long as cp is low. Any change in the input changes y but not Q for J input.

Similarly for k input circuit changes out put for the negative edge of the clock. cp when the cp is 0, the out put is 1, Then the slave latch is enabled and its out put Q is equal to the master out put y. for cp=0 the master latch is disabled when cp is high the k input sent in to master latch but when cp is low slave remains disabled. When cp is high the k input when changes the y is being changed for this but not Q.

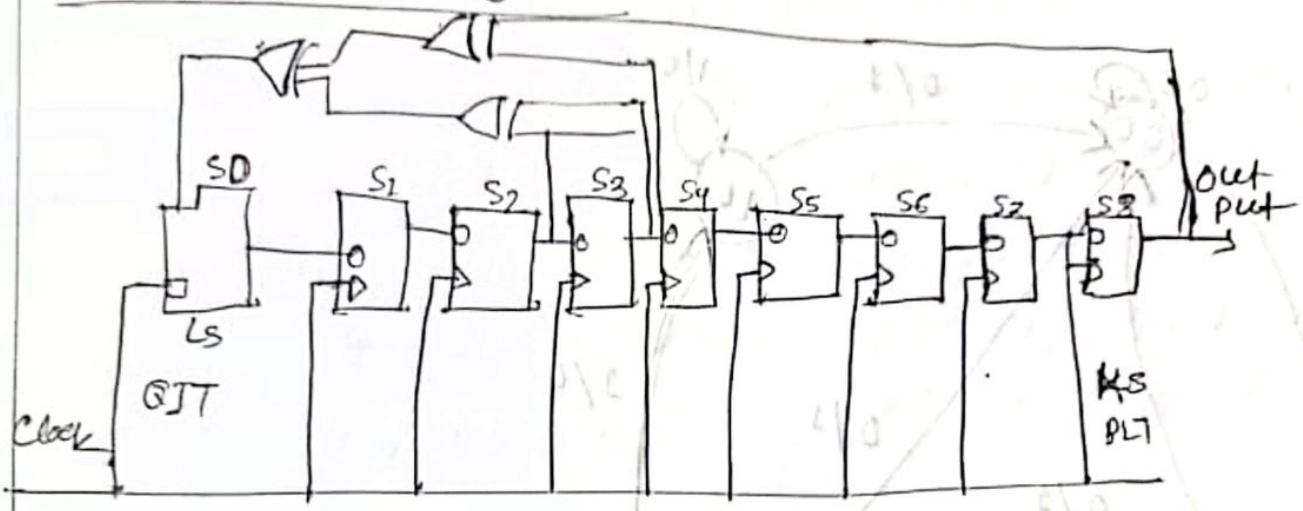
## Ans to the ques No - 2 (a)

Flowing State diagram is -



Ans to the ques No - 3 (a)

8-bit Serial register -

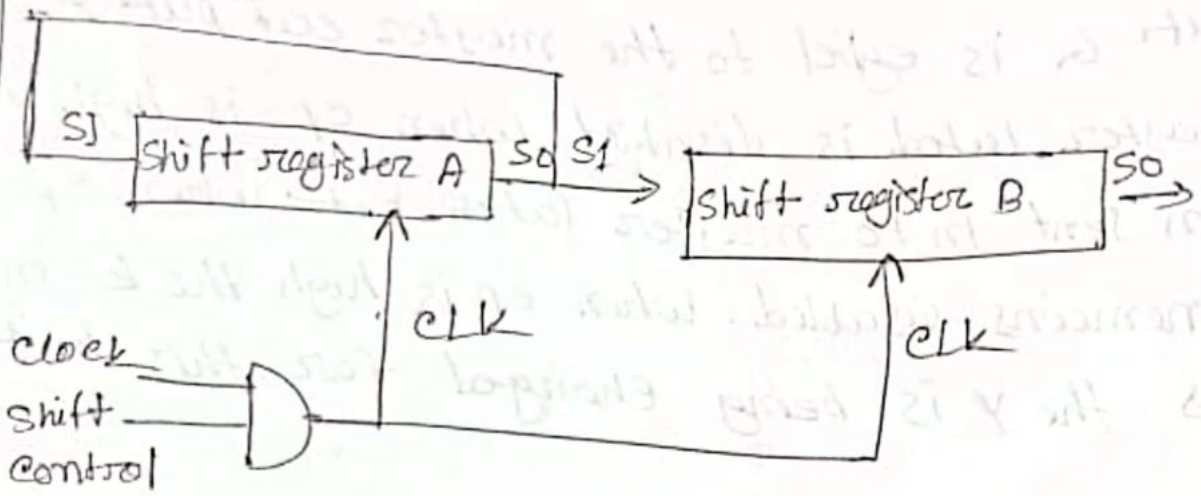



The Howing register is a 8-bit serial register. There is clock for every cell There is X-OR gate for the register Cel nomes are S0, S1, S2, S3, S4, S5, S6, S7. A the cells are connectedvia a protocal which souree to Destination register for every cell there is input which is called D and out put is called Q, by combining all the furetions the 8-bit serial register is built.

If the clock is desabled the registers turns to off mode there is X-OR furetions for the following gate.

## Ans to the ques No - 3 (b)

Serial Transfer from register Reg A to Reg B —

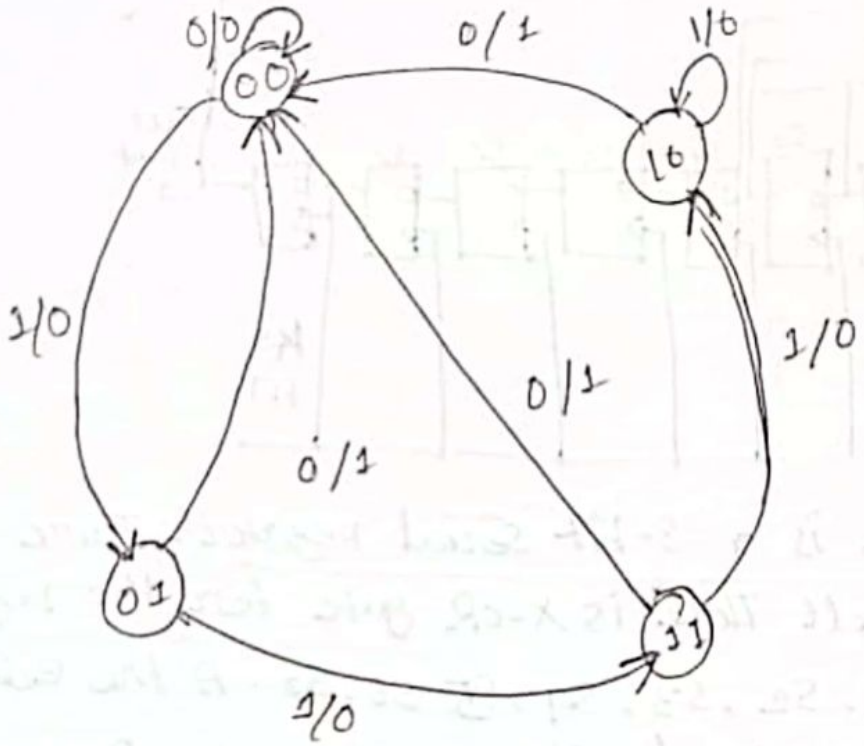



Serial - Transfer Example.

| Timing pulse | Shift Register A | Shift Register B |
|---|---|---|
| Initial value | 1 0 1 1 | 0 0 1 0 |
| After $P_1$ | 1 1 0 1 | 1 0 0 1 |
| After $P_2$ | 1 1 1 0 | 1 1 0 0 |
| After $P_3$ | 0 1 1 1 | 0 1 1 0 |
| After $P_4$ | 1 0 1 1 | 1 0 1 1 |

## Ans to the ques No - 4 (a)

State Diagram for the following question:—




| present state | | next state | | | | output | |
|---|---|---|---|---|---|---|---|
| | | $x=0$ | | $x=1$ | | $x=0$ | $x=1$ |
| A | B | A | B | A | B | Y | Y |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |

for the above transition table function are —

$A(t+1) = Ax + Bx$

$B(t+1) = \bar{A}x$

$Y(t) = (A+B)x$

for, $x=0$

$x=1$

(7)

Ans, For the above transition table formulas are,

$$A(t+1) = Ax + Bx$$
$$B(t+1) = A'x$$
$$y(t) = (A+B)x'$$

for $x = 0$, $x = 1$