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Pulse Technique

Course Code :- CSE-223

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Ans to the Q No 1

(a)

In electronics, flip-flops and latches are circuits that have two stable states that can store state information - a bistable multivibrator. The circuit can be made to change state by signals.

Example -

This simple flip-flop circuit has a set input (S) and a reset input (R). In this system, when you set "S" as active, the output "Q" would be high, and "Q" would be low. Once the outputs are established, the wiring of the circuit is maintained.

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until "S" or "R" go high, or power is turned off.

Ans to the Q No. 1

(b)

Two Types of Sequential Circuits:

a) Asynchronous sequential circuit -

1) Depends upon the input signal at any instant of time and their change order.

2) They have better performance but hard to design.

b) Synchronous sequential circuit:

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- 1) Defined from the knowledge of its signals at discrete instants of time.
- 2) Much easier to design.
- 3) Synchronized by a periodic train of clock pulses.

Ans to the Q No-2 · Ans to the Q No-2

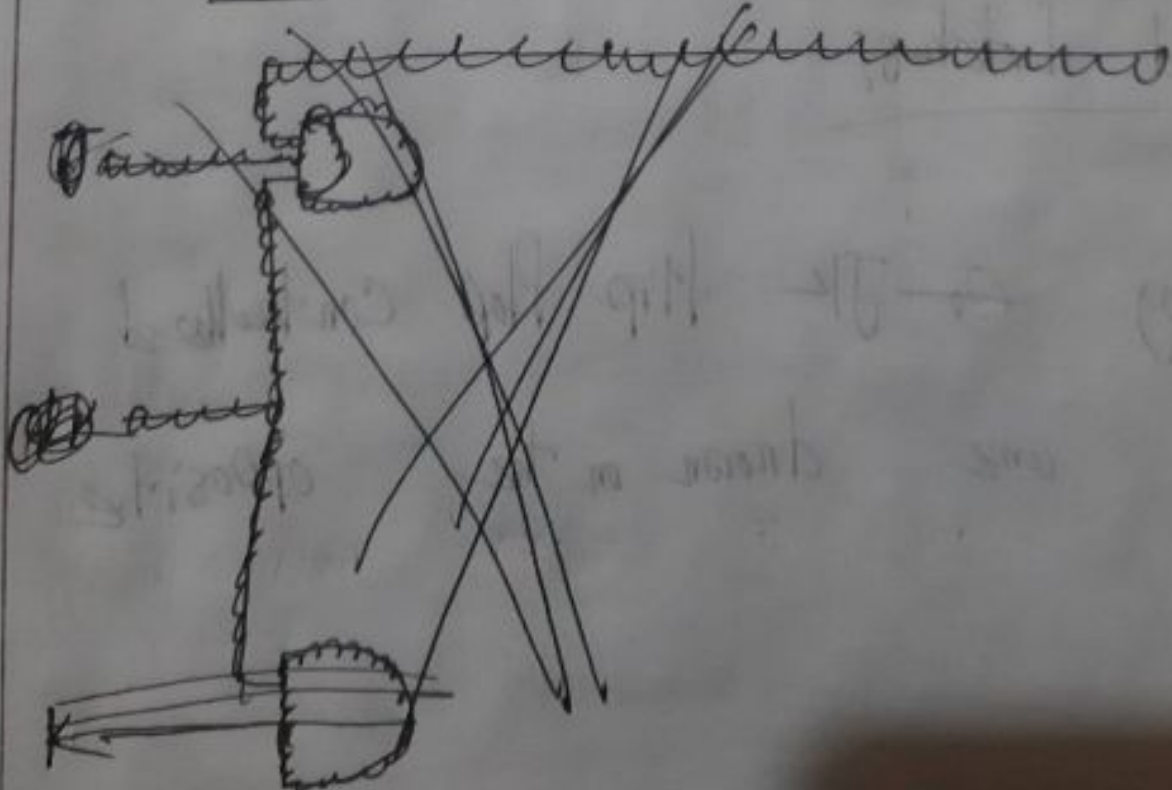
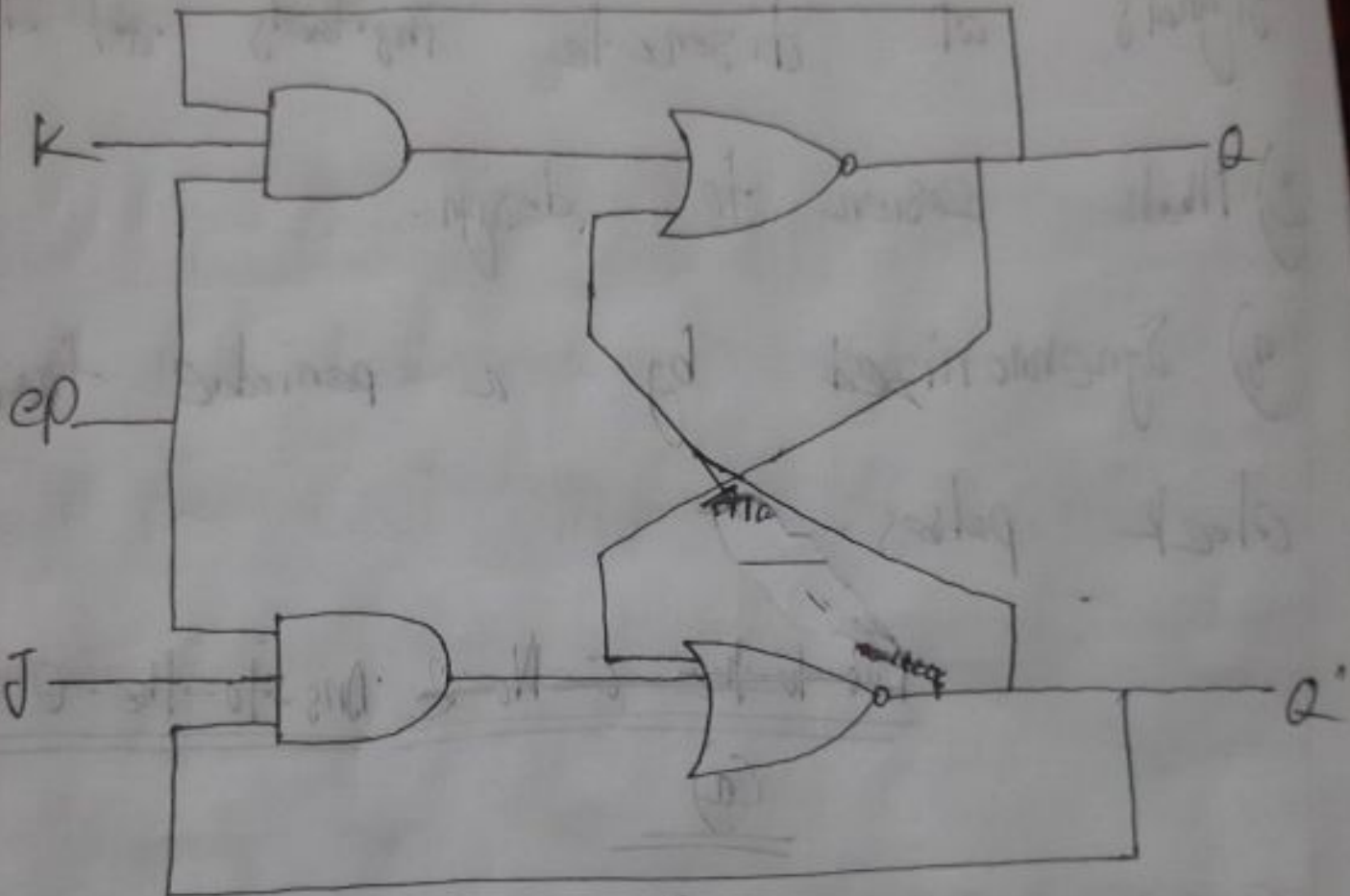
(a)

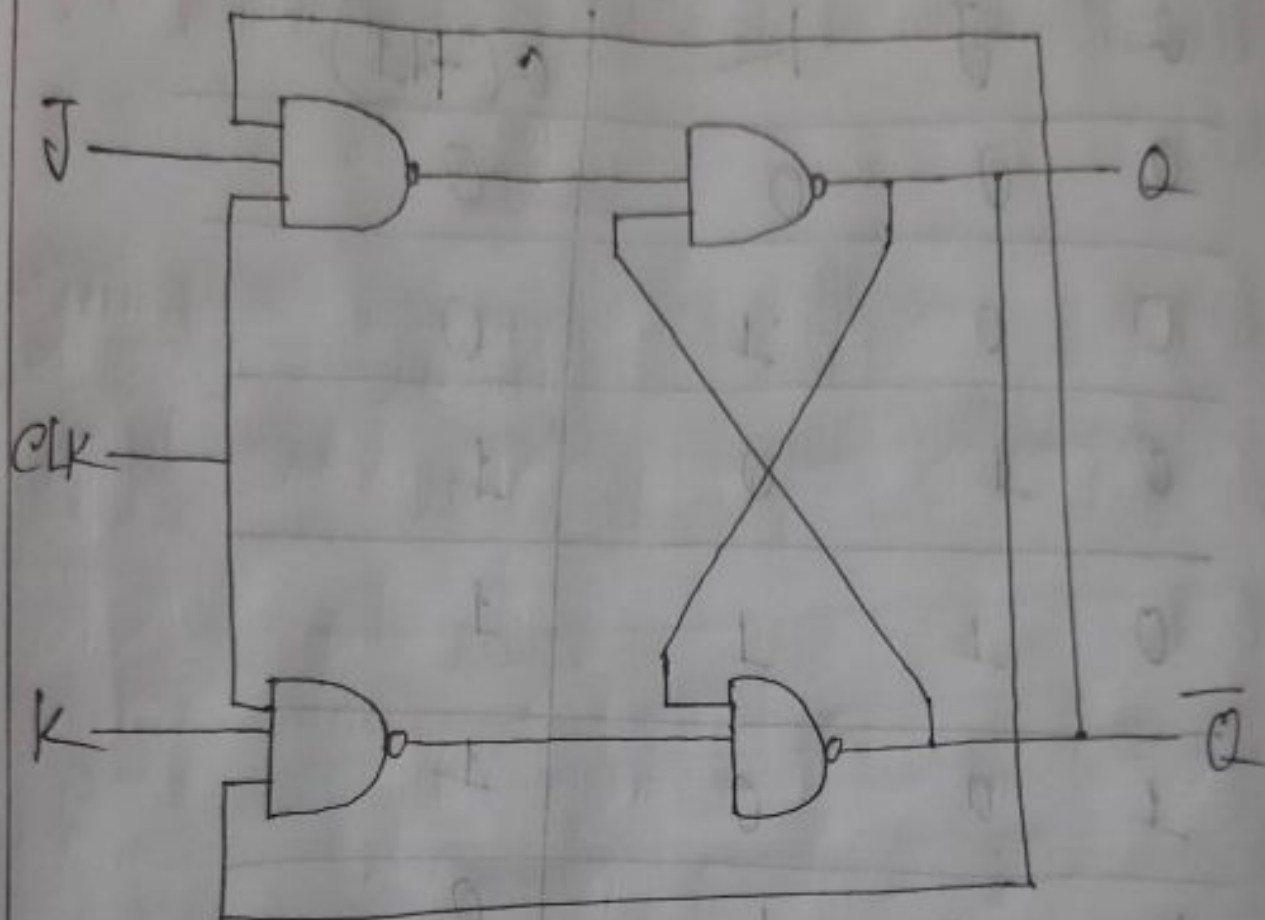
Controlled Latches:

Not Using JK flip-flop controlled Latches are drawn on the opposite

Page -

JK Latch





We can show a characteristic table to show detail about JK latch.

Here is the characteristic table -

Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

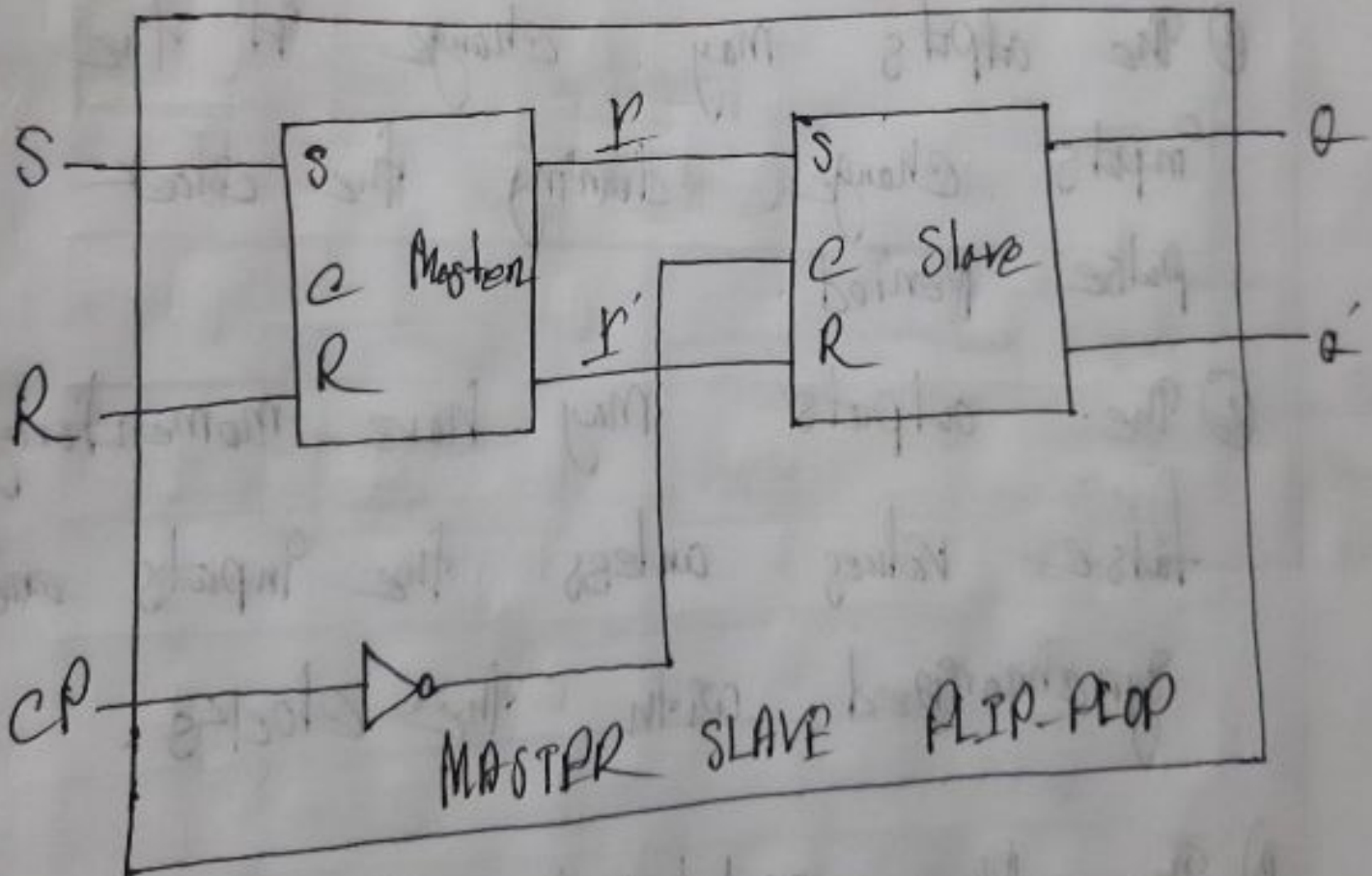
Diagram Table → Characteristic table.

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Ans-to-Que-2-No-2

(b)

Here is drawn the Master Slave SR Flip-Flop (negative edge triggered) —



Ans to Que - Q - No - 3

(a)

A) The Mealy model : the outputs are functions of both the present state and inputs.

① The outputs may change if the inputs change during the clock pulse period.

② The outputs may have momentary false values unless the inputs are synchronized with the clocks.

B) The Moore model : ~~the~~ the outputs are functions of the present state only.

① The outputs are system synchronous with the clocks

Ans to the Q No-3

(b)

(A) Mealy state machine:

Mealy Machine

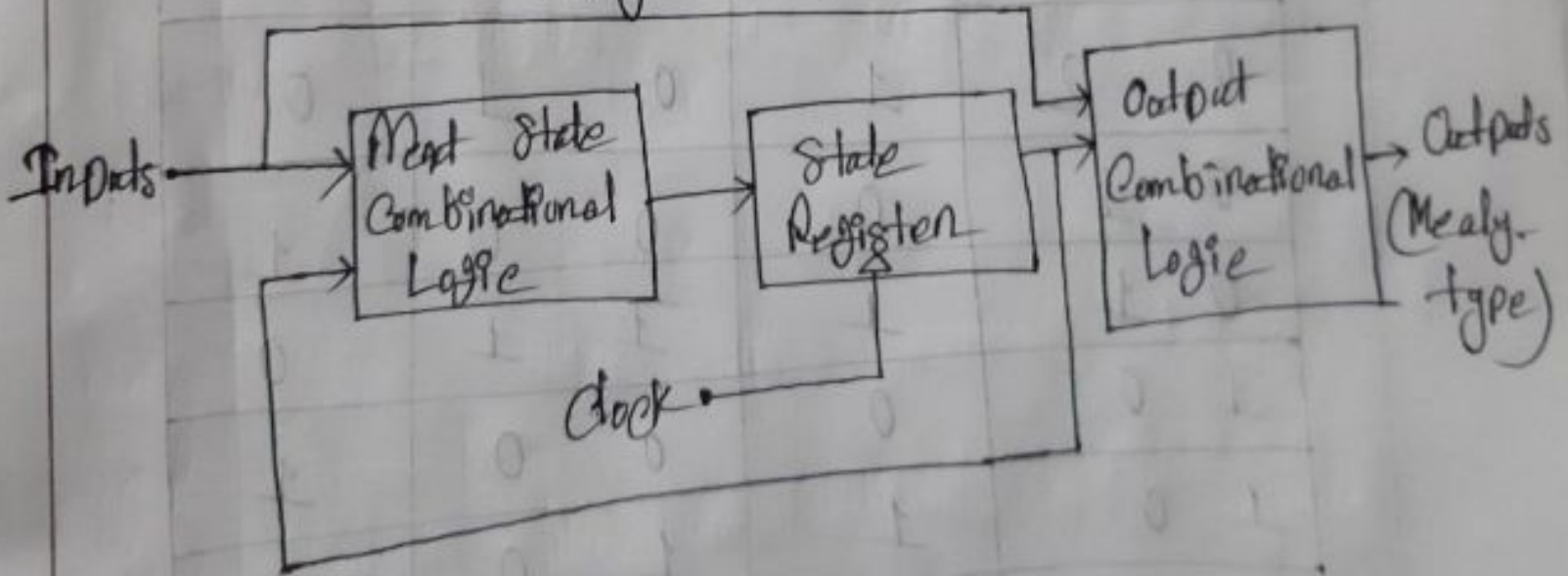


Figure: Block diagram of Mealy Machine.

Following the block diagram, there is a table of Mealy machine -

Present State		I/P		Next State		O/P
A	B	0	1	A	B	y
0	0	0	1	0	1	0
0	1	0	1	0	0	1
0	1	1	1	1	1	0
1	0	0	1	0	0	1
1	0	1	1	1	0	0
1	1	0	1	0	0	1
1	1	1	1	1	0	0

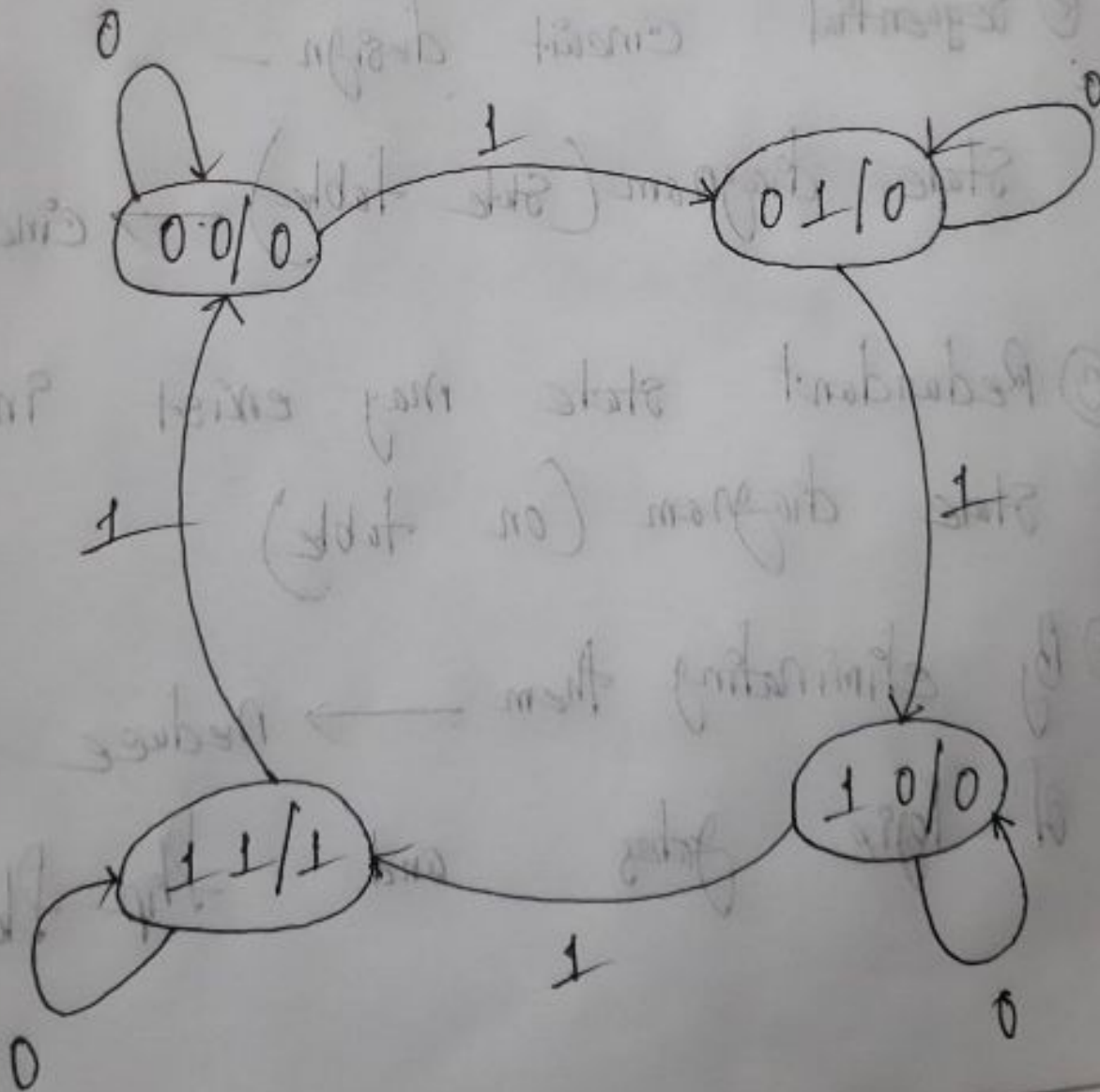
Table 1 : Mealy machine table.

Ans to the Q - No - 3

(b)

Moore State Diagram:

State / output



State Reduction

① Sequential circuit analysis —

Circuit diagram \longrightarrow state table (or state diagram)

② Sequential circuit design —

state diagram (state table) \longrightarrow circuit diagram

③ Redundant state may exist in a state diagram (or table)

④ By eliminating them \longrightarrow reduce the # of logic gates and flip-flops.