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Course Title : Digital Electronics and pulse technique

Course code : CSE-223

Ans to the Qus NO: 01 (a)

(a) Ans: In electronics, flip-flops and late has one clients that here two stable states that gun store state information -a bistable multibration.. The circuit can be made to change state by signals.

Example:

This simple flip-flop circuit has a set input (S) and a reset input (e). In this system, when you set "S" as active. the output "Q" would be high, and "Q" would be low. Once the outputs are established. The wiring of the circuit is maintained until "S" or "R" go high, or power is turned off.

Ans to the Qus NO: 01 (b)

(b) Ans:

Two types of sequential circuit:

(a) Aschonenues sequential circuit:

→ Depends when the input signal at any instant of time and their change order.

→ They have better performance but hard to design.

(5) Synchronous Sequential Circuit:

(1) Defend from the knowledge of its signals at distence instants of thime.

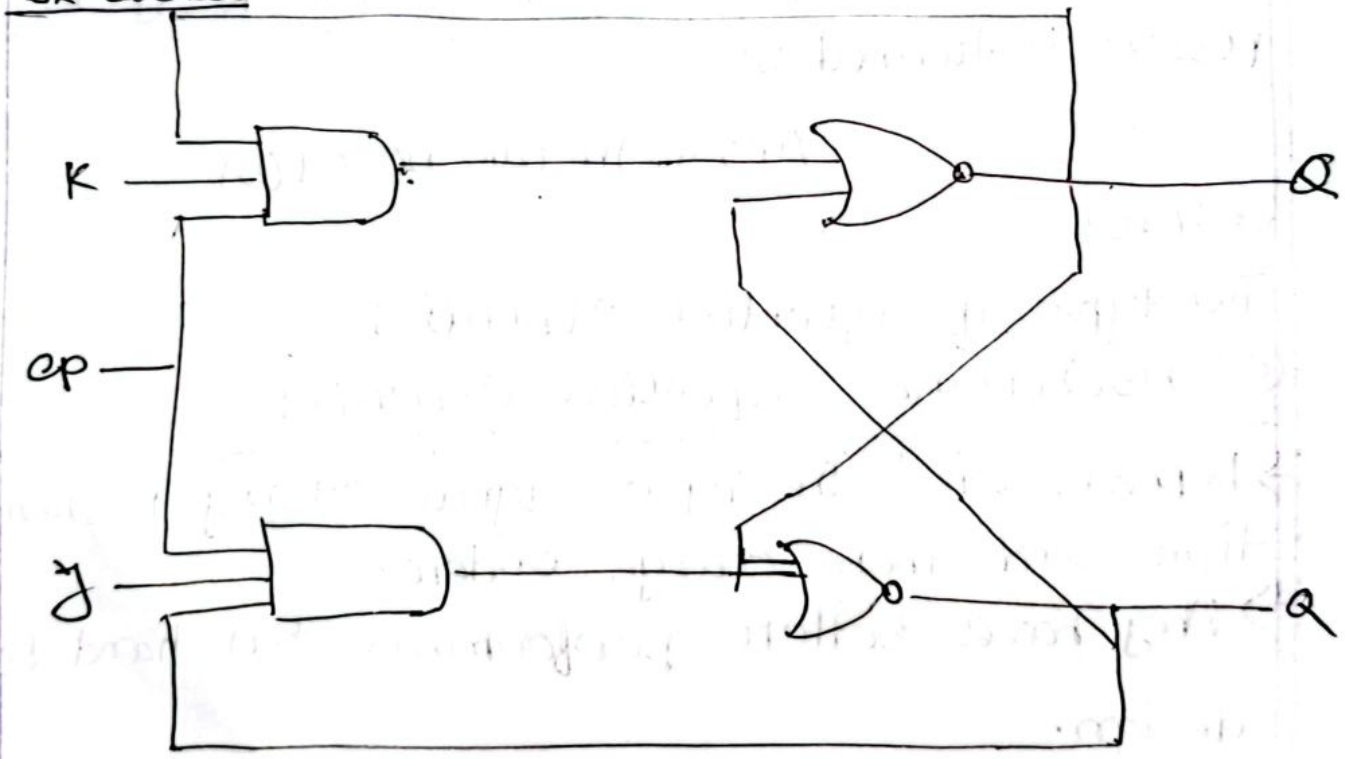
(2) Much easier to design.

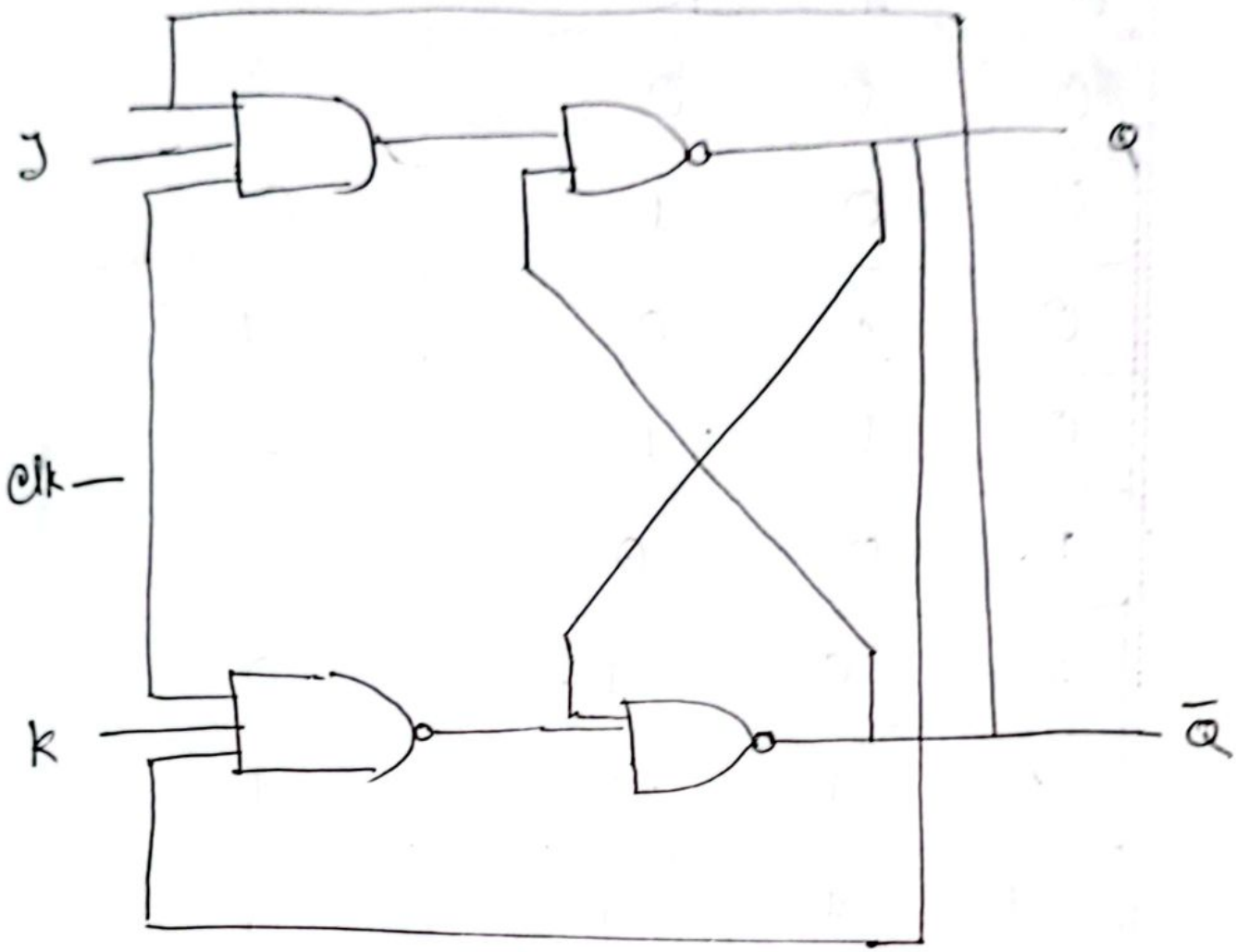
(3) Synchronized by a periodic train of clock phases.

Ans to the Qus NO:02 (a)

Ans: **Controlled latches:** Using Jk Flip-flop Controlled Latches are drawn on the opposite Page:

Jk-Lateches:





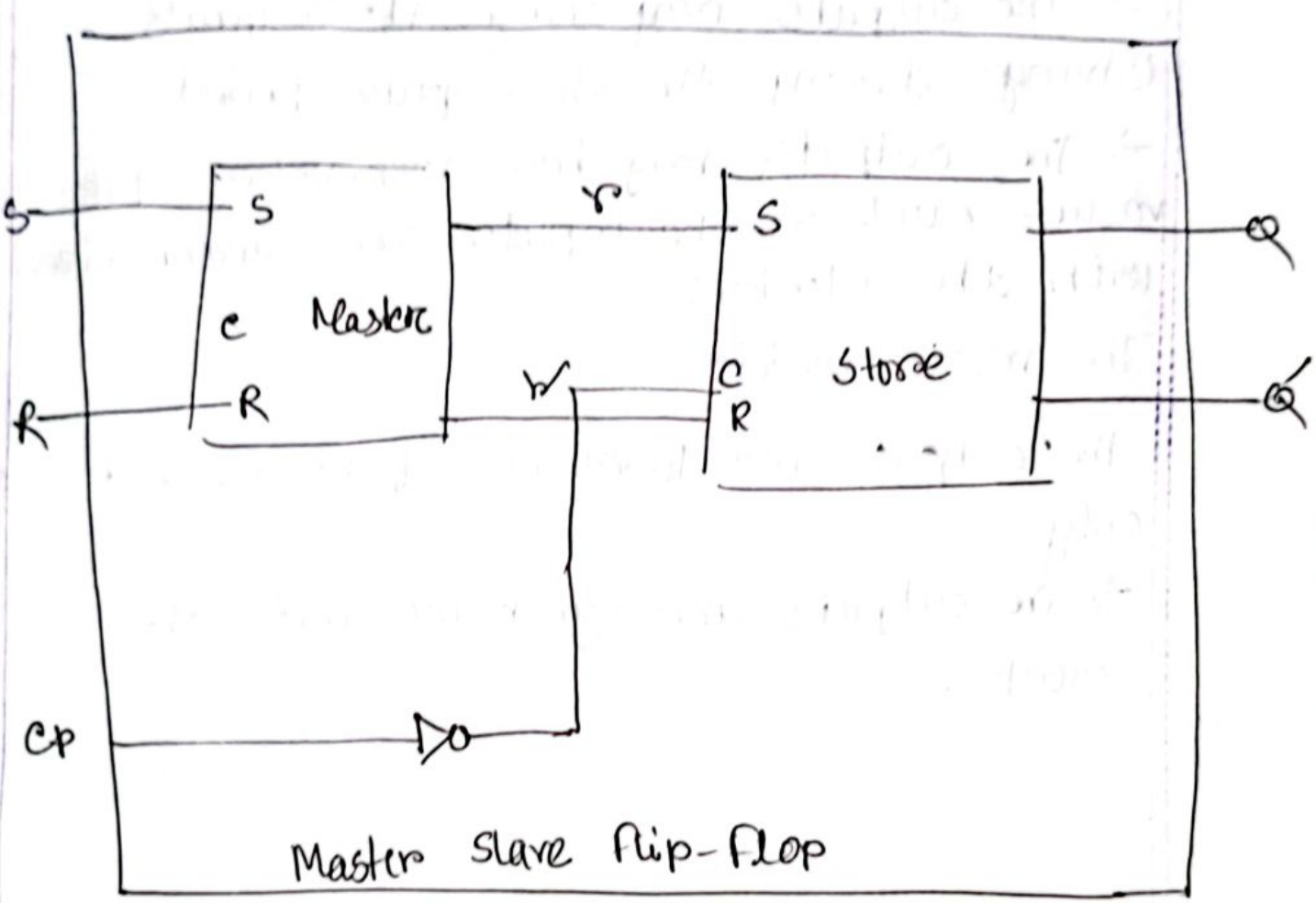
We can show a characteristic table to show detail about Jk table Here is the characteristic table.

Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Diagram table : charcharistic table.

Ans to the Qus No: 02 (5)

Ans: Here is drawn the master slave SR flip-flop (Negative edge triggared) -



Ans to the Qus No: 03 (a)

Ans: The mealy model:

The outputs are functions of both the present state and inputs.

→ The outputs may change if the inputs change during the check pulse period.

→ The outputs may have memorbry false values unless the inputs are synchronized with the clocks:

The moore model:

The outputs are functions of the present state only.

→ The outputs are synchonus with the clocks.

Ans to the Que No: 03 (b)

(b) Ans: **Mealy state machine:**

Mealy machine

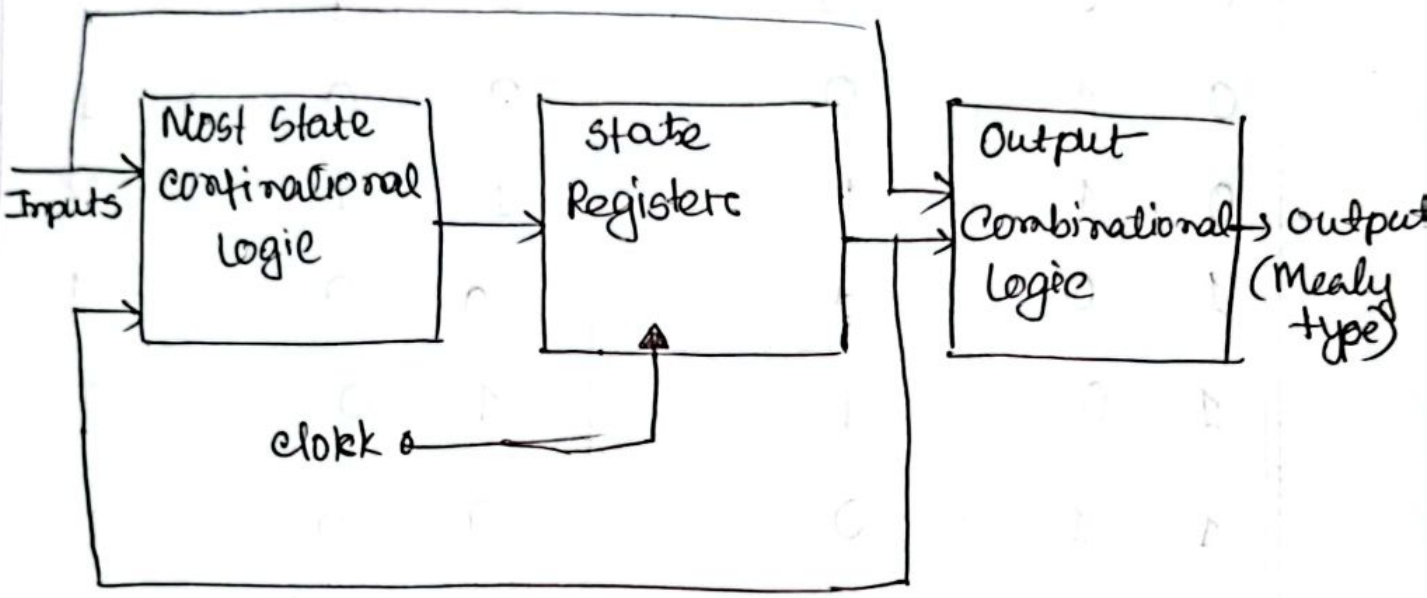


figure: Block diagram of Mealy Machine

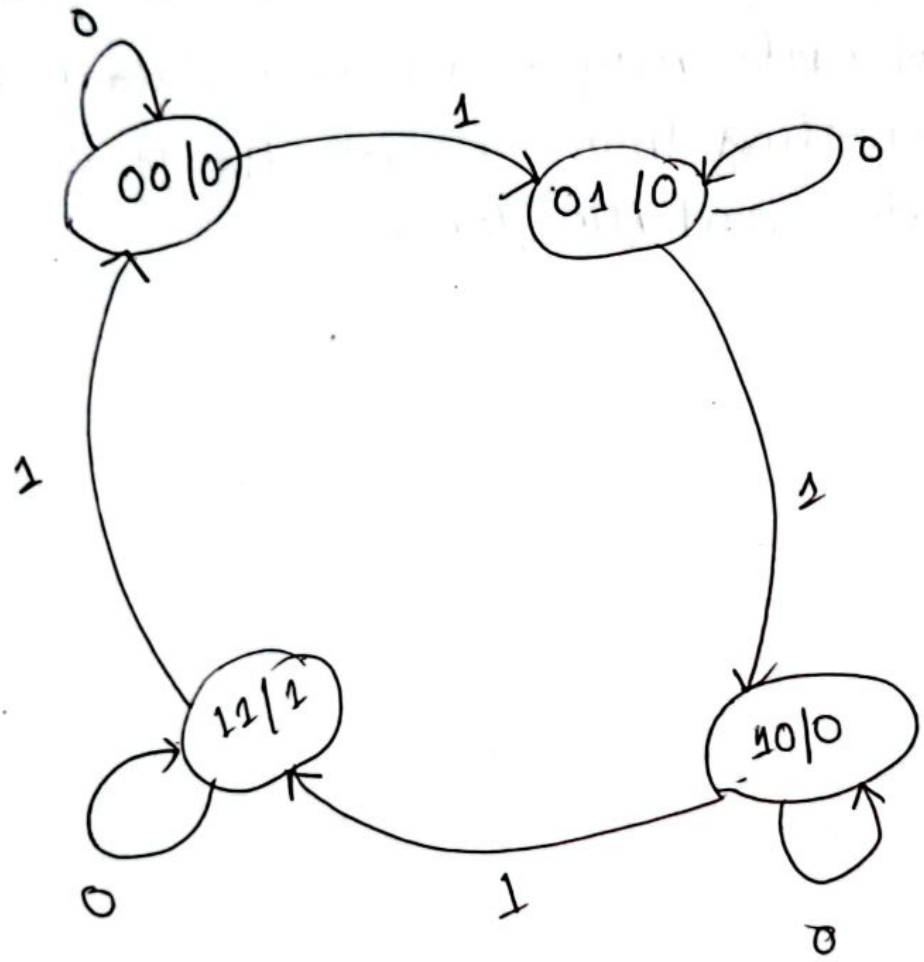
Following the block diagram here is a table of Mealy Machine.

Present state		I/p	Next state		O/p
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

Ans to the Qus No: 03(5)

Moore state Diagram:

state / output



State Rediction:

① Sequential circuit analysis –
Circuit diagram → state table (or state diagram).

② Sequential circuit design –
State diagram (state table) → Circuit diagram

③ Rederdant state may exist in a state diagram

④ By eliminating them → reduce the # of logic gates and flip-flop.