Victoria University of Bangladesh
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Mid Assessment

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Course code: CSE-223

Course Title: Digital Electronics and pulse Technique.

Ans to the ques No- 1(a)

In electronics, flip-flops and latches are circuits that have two stable states that are store state information. a bistable multivibrator. The circuit can be made to change state by signals.

Example :-

This simple flip-flop circuit has set input (S) and a reset input (R). In this system, when you set 'S' as active, the output "Q" would be high, and "Q" would be low once the output is are established. the wiring of the circuit is maintained. until "S" or "R" go high, or power is turned off.

Ans to the ques No- 1(b)

Two Types of Sequential circuits:

(a) Asynchronous sequential circuit -

① Depends upon the input single at any instant of time and their change order.

② my have better performance but mand to design.

(b) Synchronous sequential circuit:

① Defined from the knowledge of its singles at discrete instats of time.

② much easier to design.

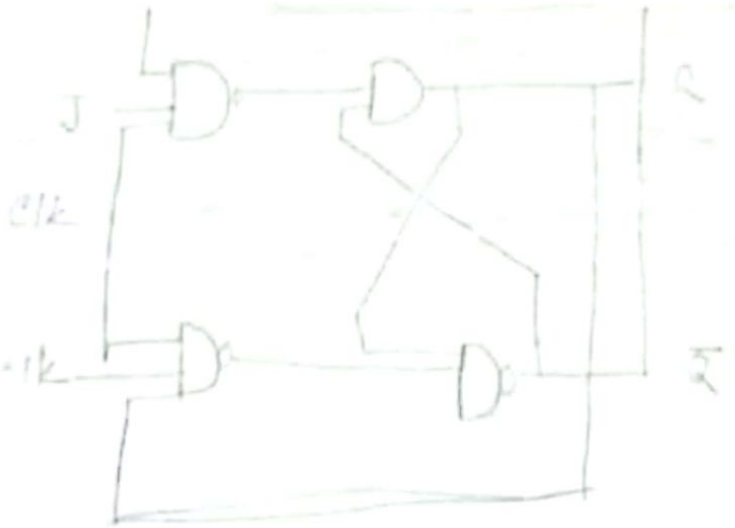
(3) Synchronized by a periodic train of clock pulses.

Ans to the ques No-2(a)

Controlled Latches:

Using JK flip-flop Controlled latches are drown on the opposite page-

JK latch



(3)

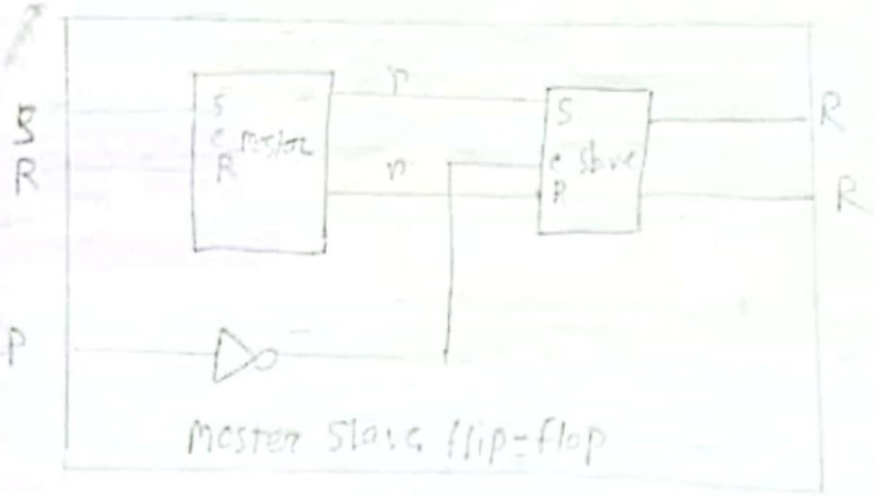
We can show a characteristic table to show detail about JK letch. Here is the characteristic table –

Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Diagram Table :- Characteristic Table.

Ans to the ques No- 2 (b)

Here is drown the master slave SR flip-flop (negative edge thiggered) –



Ans to the ques No-3(a)

A) The mealy model; The alputs are functions of both the present state and inputs.

① The alputs may change if the inputs change during the clock pulse period.

② The alputs may have momentary false values unless the inputs are synchronized with the clocks.

B) The moore model: The outputs are functions of the present state only

① The alputs are synchronous with the clocks.

Ans to the ques No-3-(b)

A) Meady state machine:

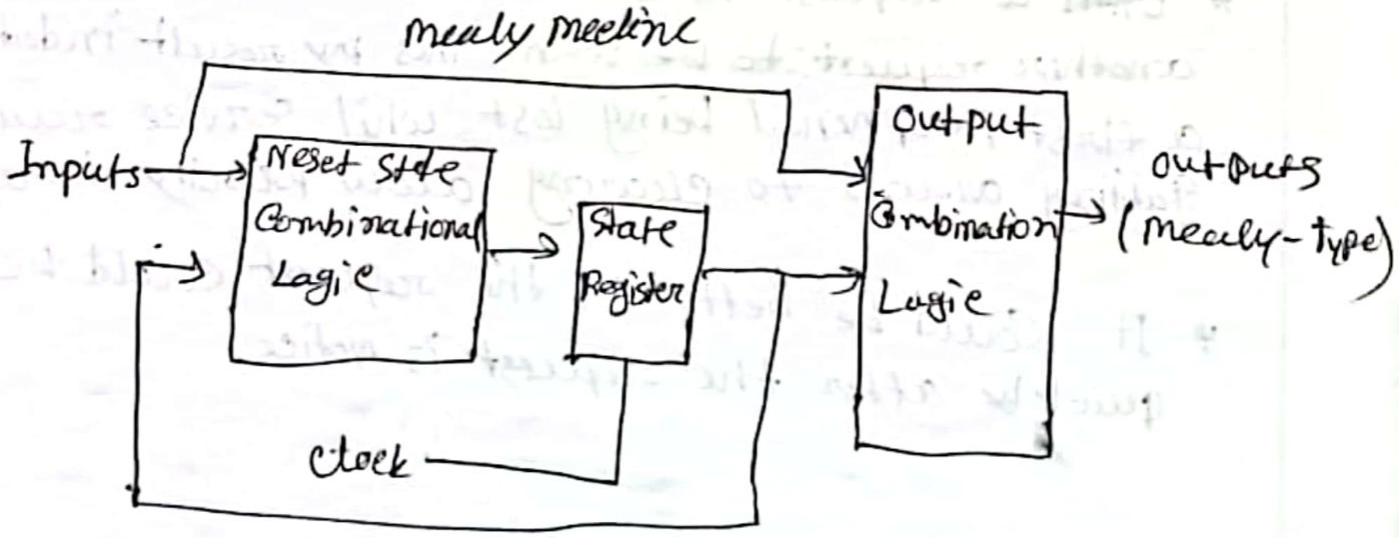


figure:- Block diagram of mealy machine

(b)

following the block diagram here is a table of meady machine meely

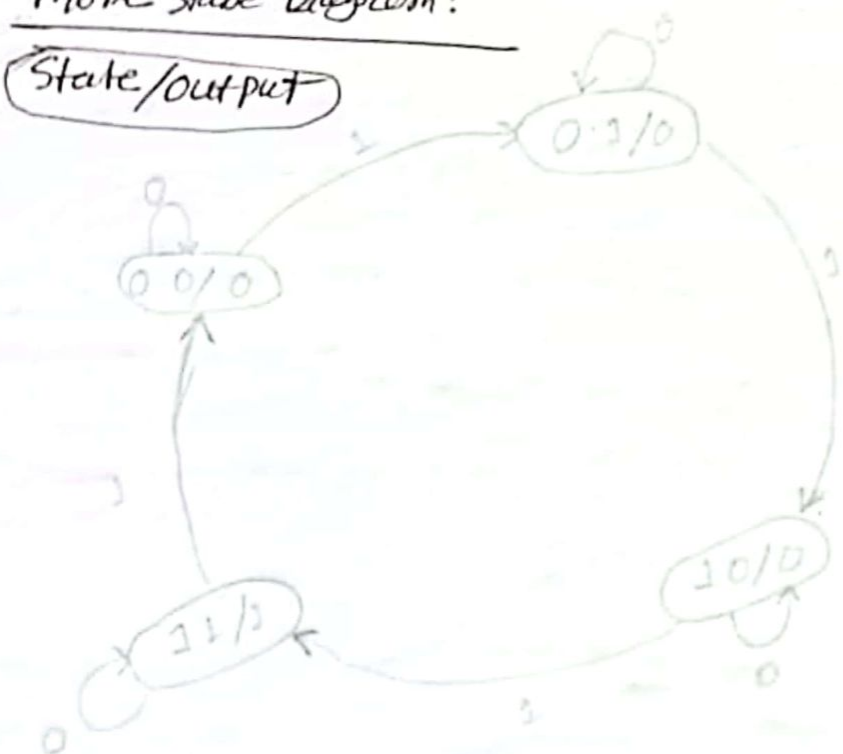
Present state		I/p	Next state		O/P
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

Ans to the ques No - 3(b)

(c)

More State Diagram:

State/output



State Redetion

① Segention Cineuit crelysis —

Cineuit diagram ⟶ state table (on state diagrem)

(6)

(2) Sequential circuit design —
State diagram (state table) → circuit diagram

(3) Redundant state may exist in a state diagram (or table)

(4) By eliminating them → reduce the # of logic gates and flip-flops.