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Course code: CSE-223
Course title: Digital Electronics and pulse Technique.
"Mid Assessment"

Ans to the Q.NO: 01

(a) In electronics, flip-flops & latches are circuits that have two stable states that can store state information - a bistable multivibrator. The circuit can be made to change state by signals.

Example :- This simple flip-flop circuit has a set input (S) & a reset input (R). In this system when you set 'S' as active, the output 'Q' would be high, & 'Q' would be low once the Output is established, the writing of the circuit is maintained, until 'S' or 'R' go high, or power is turned off.

(b) Ans: Two types of sequential circuits :-

(1) Asynchronous sequential circuits —

(a) Depends upon the input signal at any instant of time & their change order.

(b) May have better performance but hard to design.

(2) Synchronous sequential circuits :

(a) Defined from the knowledge of its signals at discrete instants of time.

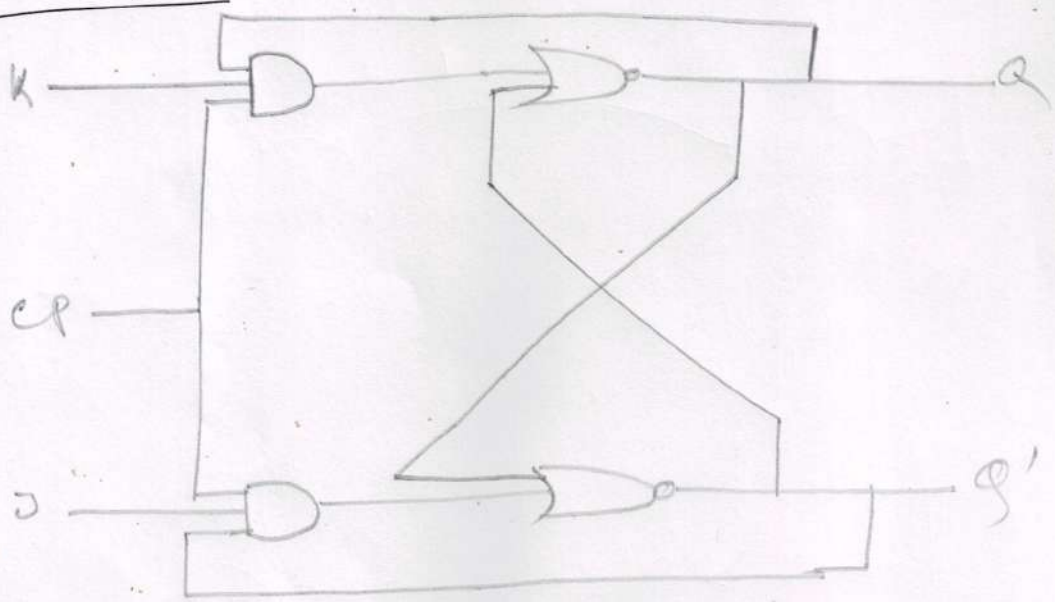
(b) Much easier to design.

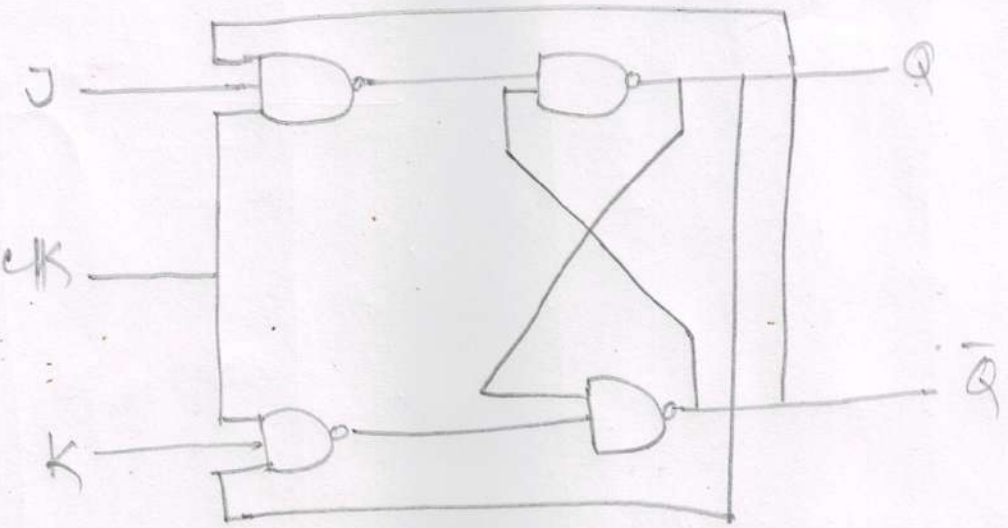
(c) Synchronized by a periodic train of clock pulses.

Ans: the Q: NO: 02

(a) Controlled latches: Using JK flip-flop controlled latches are drawn on the ~~opposite~~ page.

JK latch –





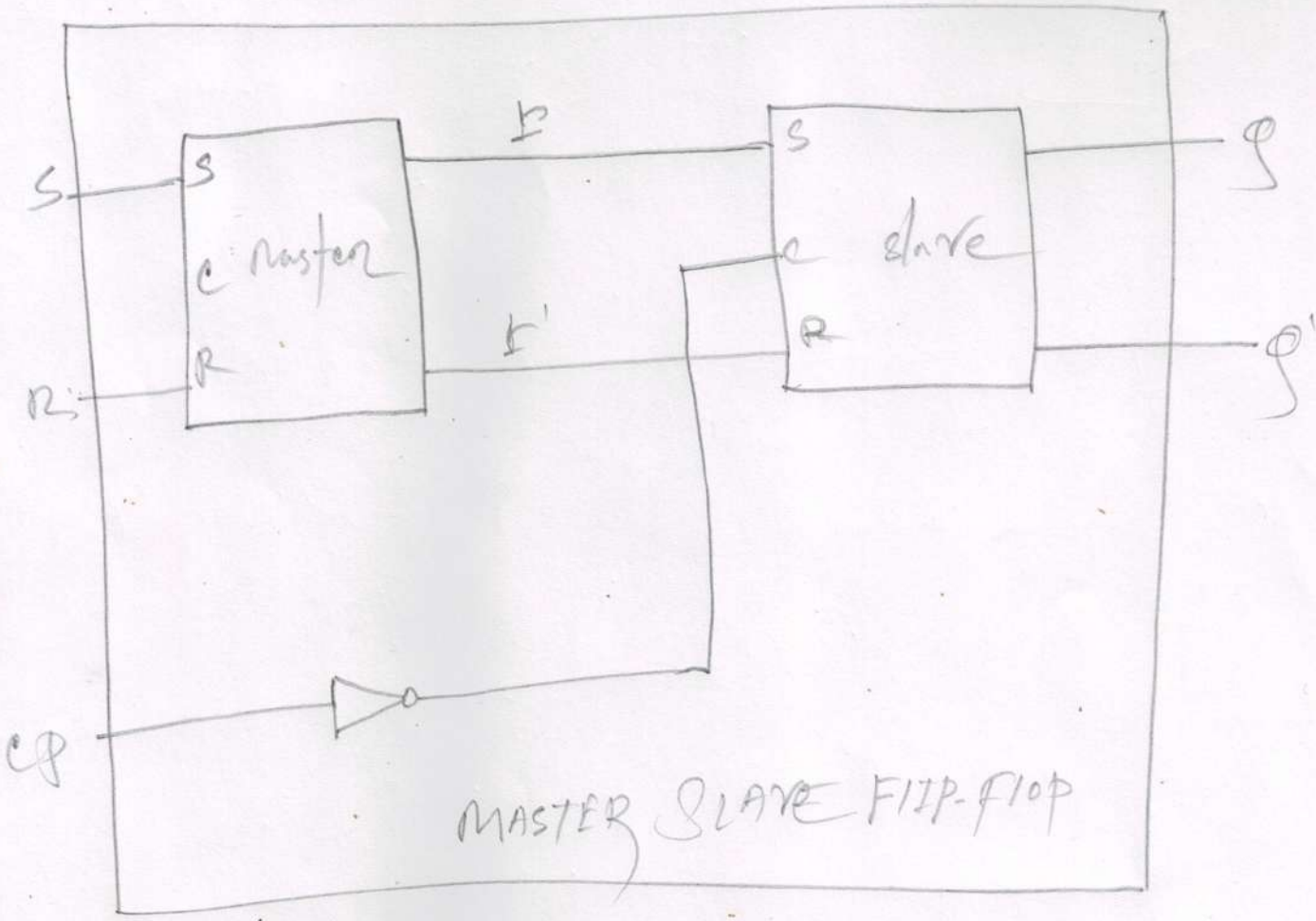
We can show a characteristic table to show detail about JK letch. Here is the characteristic table –

Q	J	K	Q (t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Diagram :- characteristic table.

Ans: to the Q. no: 02

(b) Here is drawn the master slave SR flip-flop (negative edge triggered)



Ans: for the Q: NO: 03

(a)

(A) Ans: The mealy model: the outputs are functions of both the present state & inputs.

(1) The outputs may change if the inputs changes during the clock pulse period.

(2) the Outputs may have momentary false values unless the inputs are synchronized with the clocks.

(B) the moore model: the Outputs are functions of the present state Only.

(1) the outputs are synchronous with the clocks.

Ans: the q: NO: 03

(b)

Mealy state machine:

Mealy machine

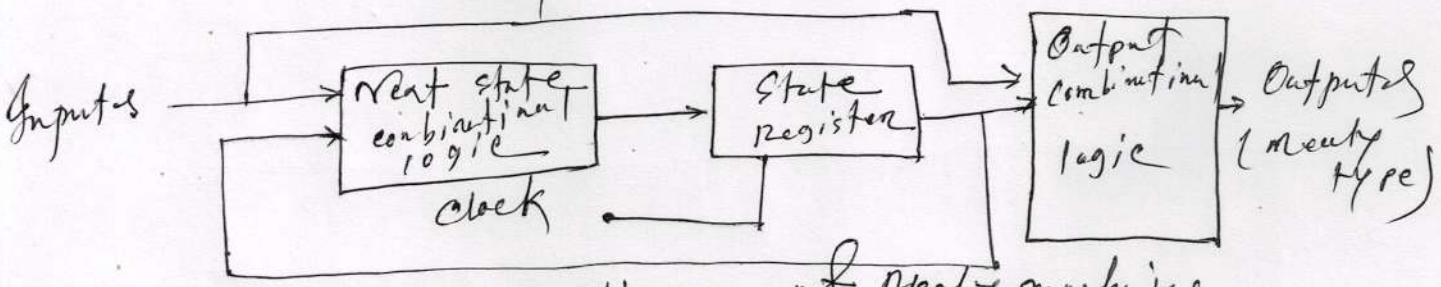


Figure: Block diagram of Mealy machine

following the block diagram here is a table of Mealy machine-

Mealy

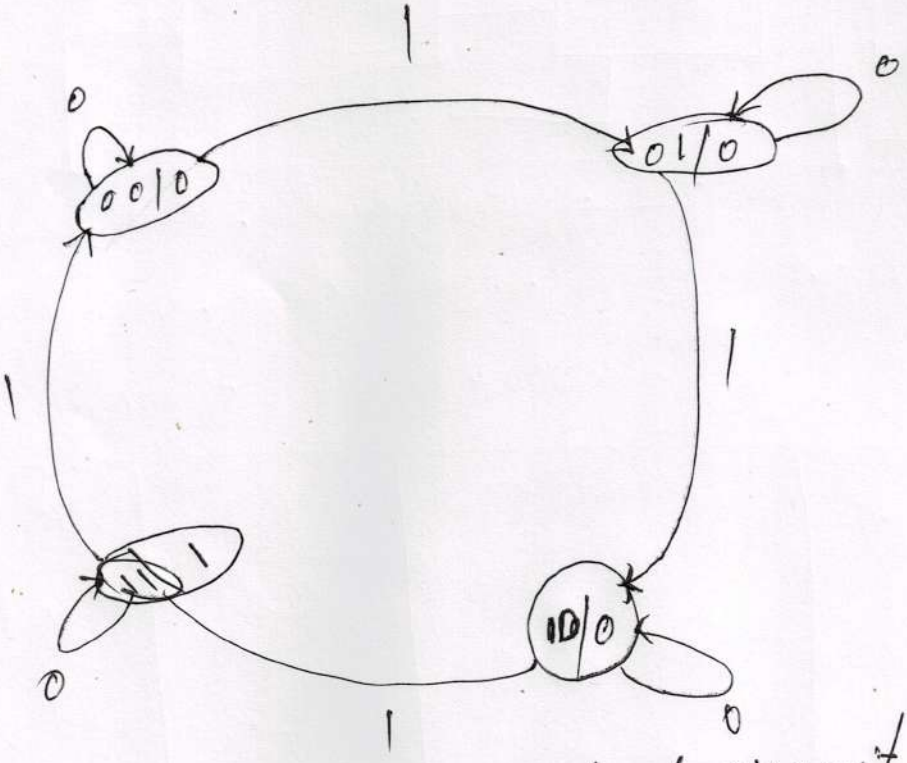
Present state		I/P	Next state		O/P
A	B	x	A	B	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

Table-1: Mealy machine table.

Ans! to the! Q! NO! 3

(c) Moore State Diagram:

State/Output



State Reduction: (1) sequential circuit analysis — circuit diagram ⟶ state table (or state diagram)

(2) Sequential circuit design — State diagram (state table) ⟶ circuit diagram.

(2) Redundant state may exist in a state diagram (or table)

(4) By eliminating them — reduce that the # of logic gates & flip-flops.