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Course- Computer Organization & Assembly Language.
Course Code- CSE-233.

Answer to the Question No — 1

(A) Answer: Full Adder Logic gate: Full Adder is the adder that adds three input and produces two Outputs. The first two inputs are A and B And the third input is an input carry as C-IN. The Output carry is Designated as C-out and the Normal Output is designated as S which is the Sum. The C-Out put is also known as ~~that~~ they majority 1' detector, whose output goes high when more then input together to Create a byte-wide adder and cascade the carry bit from one Adder and cascade the carry bit from ~~and~~ one adder to Another. We used a full adder because when a carry in bit is available, another 1-bit adder must be used since a-1 bit half adder does not take carry in bit. A 1 bit full adder three operants and generates 2 bit Result.
When the Addition of two bainary digits is performed then sum is genarated. if it consists of two digit in the Out put then the MSB bit is Referred to as carry. This is treated as the third bit in the process of Addition.

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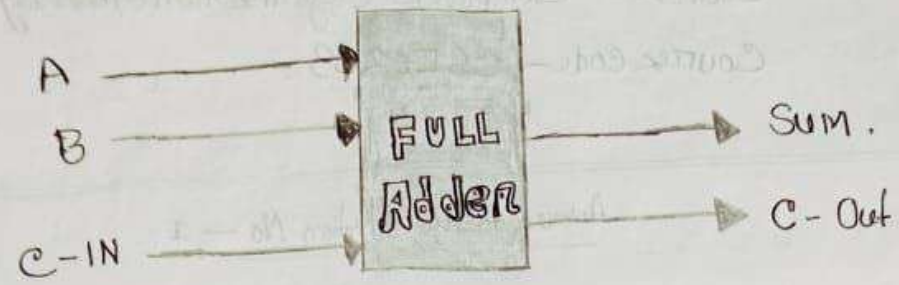
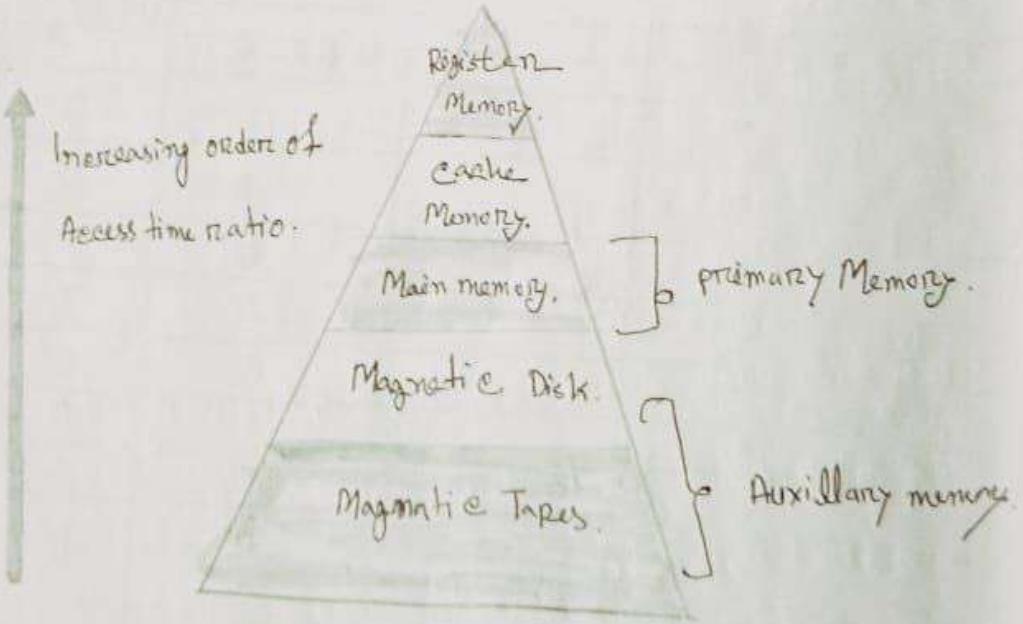


** Full Adder Truth Table:

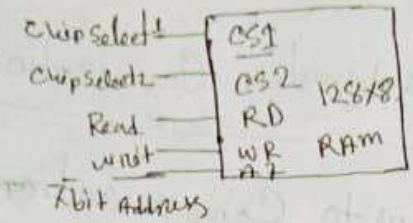
INPUT			OUTPUT	
A	B	C-IN	Sum	C-Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Answer to the Question- No- 2

(A) Answer: Memory Sub system organization: The memory is divided into cells, and each of them is identified by a unique number called an Address. When the cpu wants to read or write an Address, it generates Control signals such as 'read' and 'write' which each cell can identify.



(b) Answer:



If we see RAM physically then we notice that RAM is made up of a few chips, we can design the required RAM size using Basic RAM chips. We can observe a basic RAM chip follows.

CS1: for chip select 1, the value should be 1

CS2: for chip select 2, the value should be 0.

Read and write: used for upcoming signals.

if we have n bit Address and m bit word then our RAM size will be $2^n \times m$.

Example. n = 7 bit, m = 8 bit

RAM size = 128 × 8

given, Basic RAM size = 128 × 8.

Required RM size = 512 × 8

To design RAM size of 512×8 from 128 × 8, here are calculation we need to first.

① Number of chips Required:

Number of chip Required = Desired RAM size / Basic RAM size

= 512×8 / 128×8

= 4 chips.

(2) Address Bits: Required size is 512×8

$$512 \times 8 = 2^9 \times 8$$

Therefore, 9bit address is required.

(3) Decoder size: If the number of word is increasing there will be a need for a decoder. In this case number of word is increasing (from 128 to 512)

Size of decoder = number of time word increasing

$128 \rightarrow 512$

word increased by 4 times.

Decoder size $= 2 \times 4$.

pictoral Description (Design 512×8 RAM)

—— x ——

Answer to Question No - 3

(a) Answer: A Model of I/O subsystem Organization: Input and Output (I/O) Devices Allow us to Communicate with the Computer System. I/O is the transfer of Data between primary Memory and various I/O peripherals. Input devices such as keyboard mice, card readers, scanner, voice recognition System and touch Screen enable us to enter Data into the Computer.

The I/O Subsystem of a Computer provides efficient mode of Communication between the Central System and the Outside Environment. It Handles all the input - Output operations of the Computer System.

We can classify input/output ports into four categories Based on the CPU's ability to read and write data at a given port address. These four categories are - Read-only ports write-only ports, Read/write ports and dual I/O ports.

P.T.O.

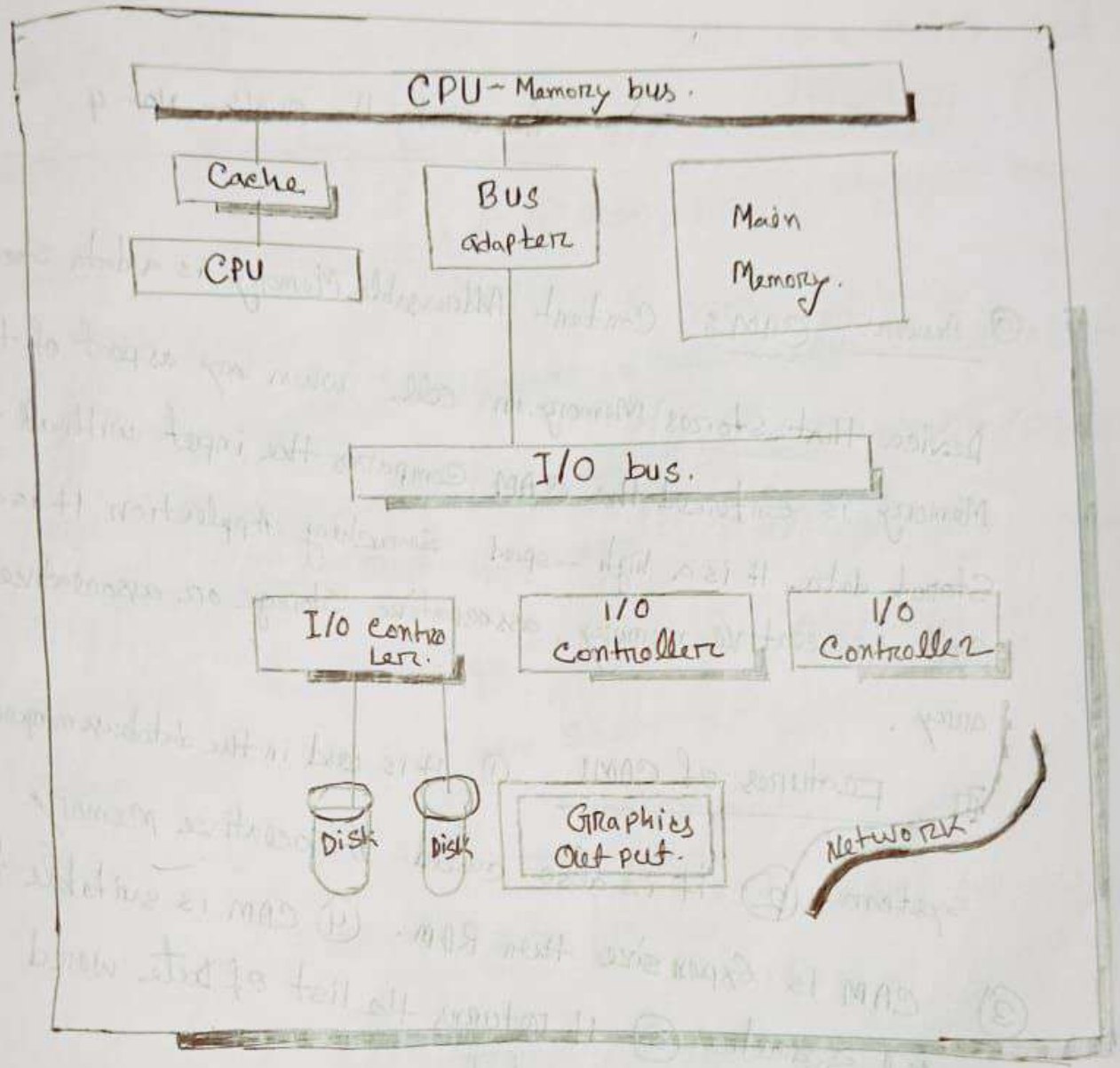


Fig: A mode of I/O subsystem organization.

Answer to the Question No - 4

(a) Answer: CAM: Content Addressable Memory is a data storage Device that stores Memory in cell. when any as part of the Memory is Entered the CAM compares the input with all the Stored data. It is a high - speed searching Application. It is also Call associative memory, associative storage or associative array.

(i) Features of CAM: (1) It is used in the database management system (2) it is also called Associative Memory (3) CAM is Expensive than RAM. (4) CAM is suitable for parallel search. (5) It returns the list of Data word Address that was ~~all~~ selected.

(ii) working of CAM: (1) Content - Addressable Memory (CAM) is a silicon chip for amazingly quick yet unmistakable kinds of memory.

(2) Queries utilizing a CAM is theoretically Like a cooperative exhibit rationale in data structures yet the yield is very streamlined.

p.t.o

③ At the point when the key is passed to a CAM sub framwork, it Restores the related incentive to that key. Because a "key → esteem" pair is made that can be Retrieved further.

④ The most significant elements is that Query of section in a CAM can be performed in a solitary clock cycle in the silicon.

⑤ A RAM module that requires various clock cycles to make a solitary Memory brings a CAM cell in the requires chip that comprises two SRAM cells.

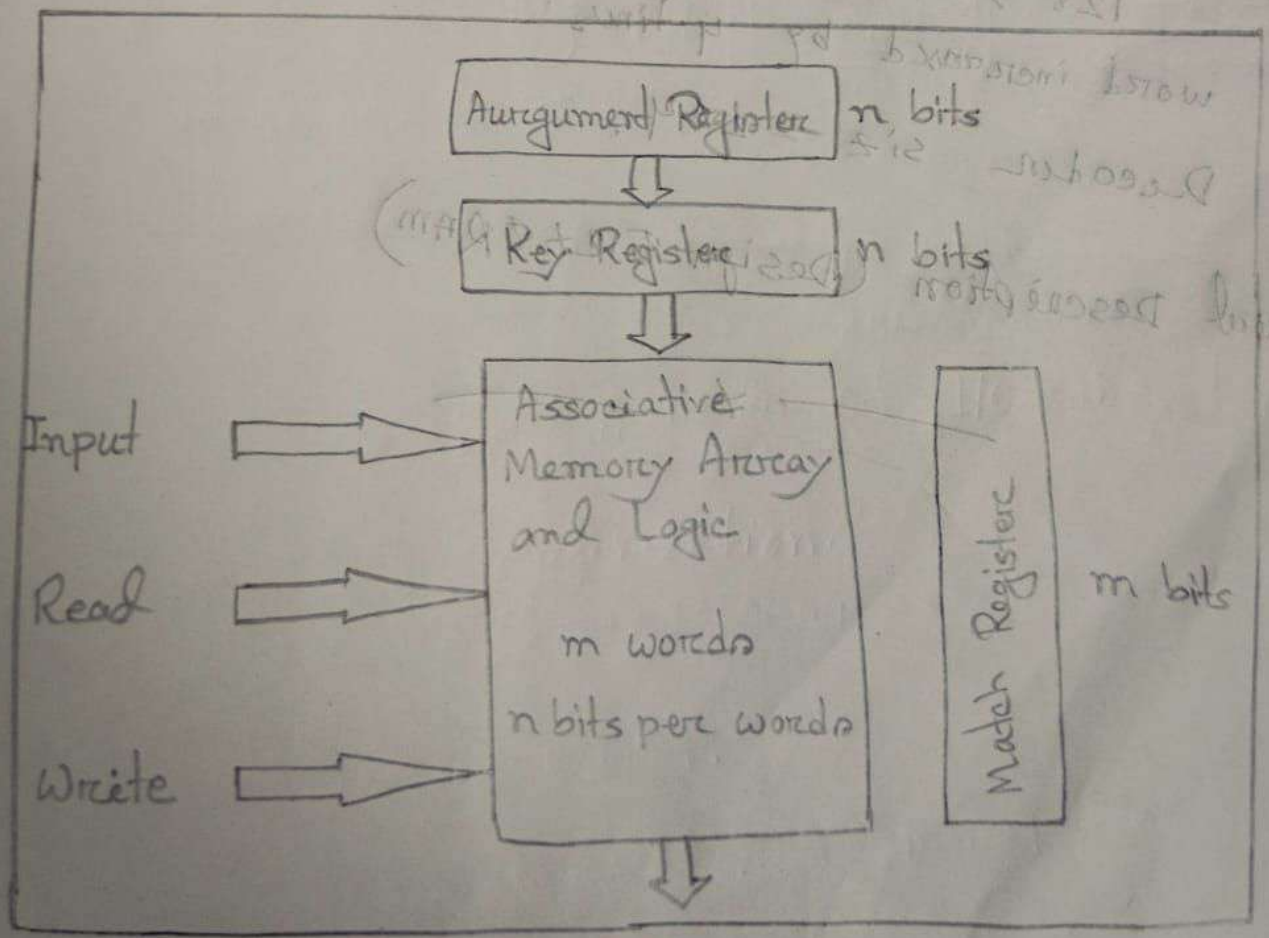


Fig: Content-addressable memory