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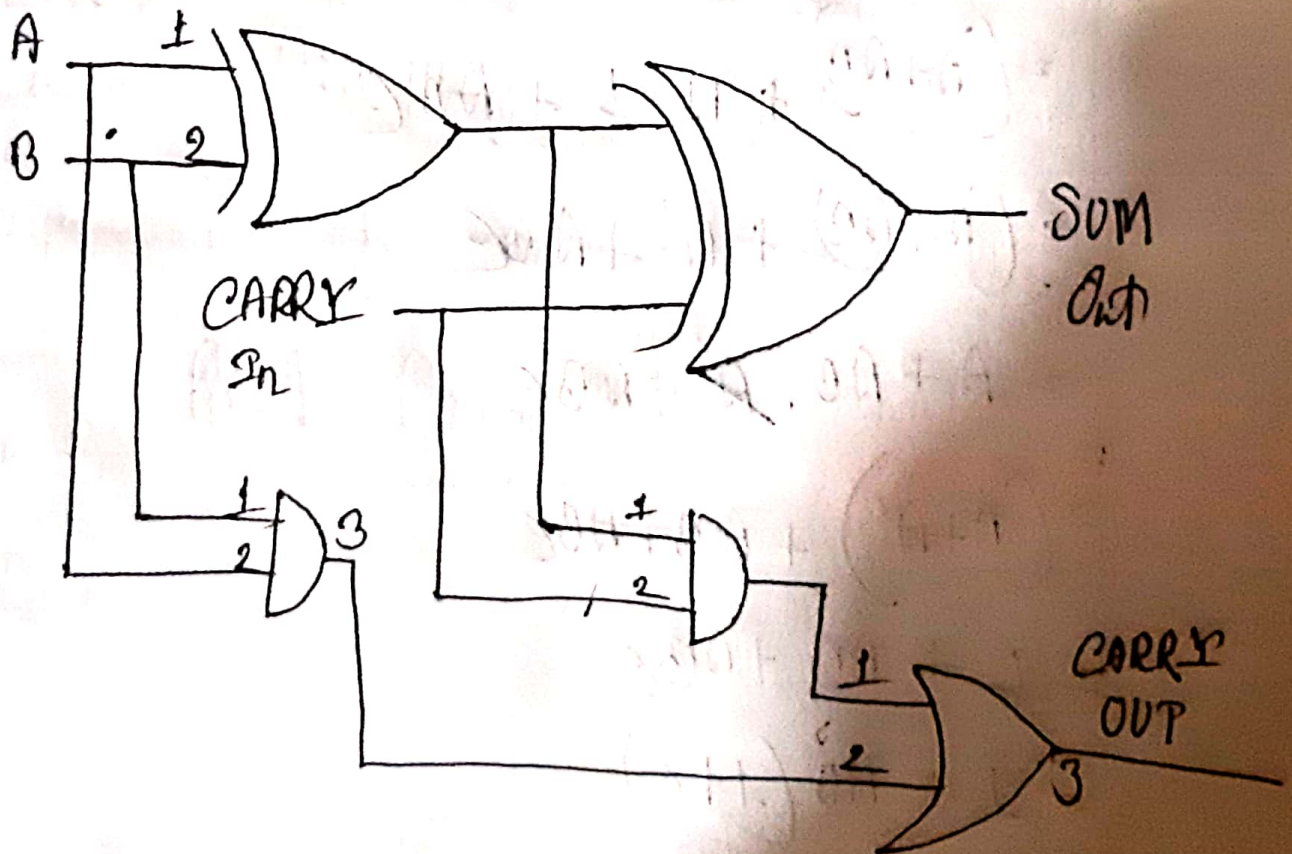
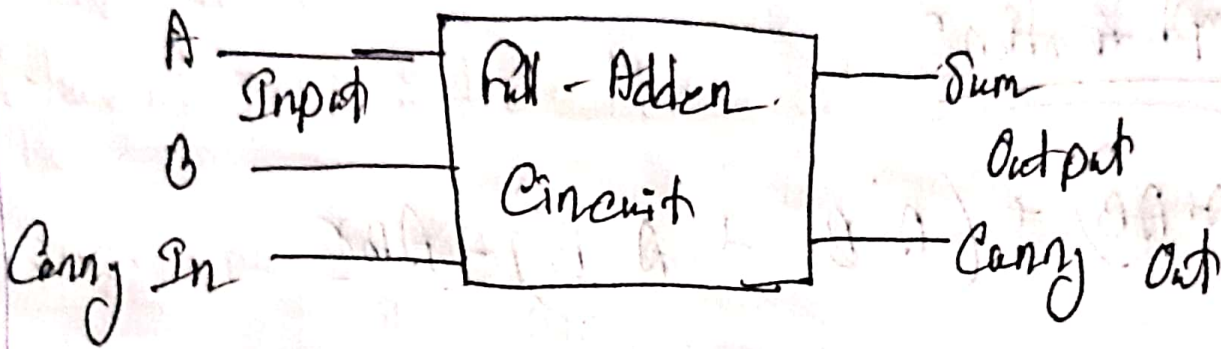
Course Title :- Computer Organization and
Assembly Language

- "Final Exam"

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Ans - to the Q - No - 1 (a)

Full Adder using basic gate:-



2

Ans to Que Q No - 1

(b)

Simplification:

$$(A+AB)' + (A'B' + A'B) + ABC$$

$$= (A+AB)' + (A'(B'+B)) + ABC$$

$$= (A+AB)' + A' \cdot 1 + ABC$$

$$= (A+AB)' + A' + ABC$$

$$= A + AB + A' + ABC$$

$$= (A+A') + AB + ABC$$

$$= 1 + AB + ABC$$

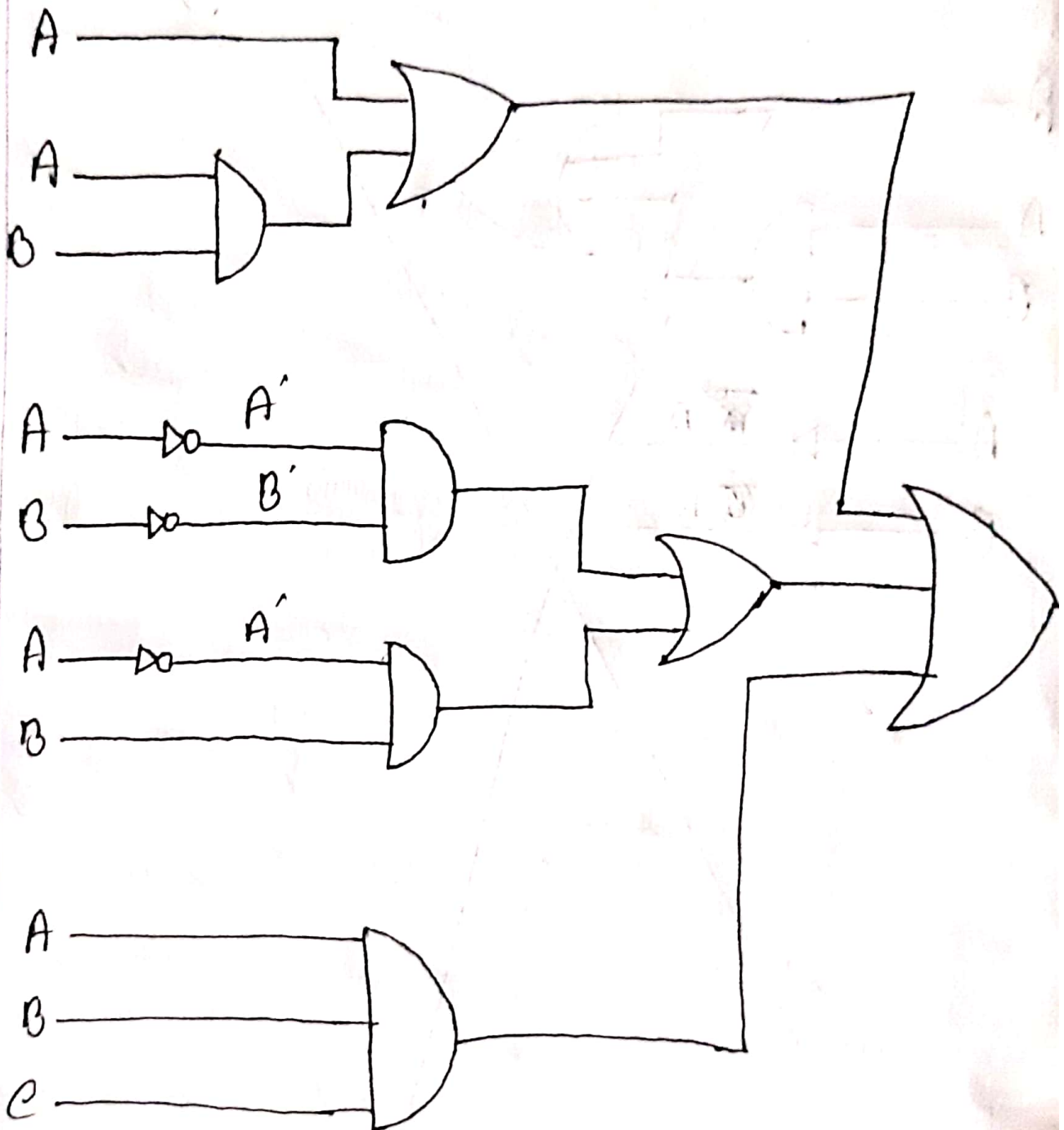
$$= 1 + AB(1+C)$$

$$= 1 + AB \cdot 1$$

$$= 1 + AB \text{ Ans.}$$

3

Circuit: $F = (A+AB) + (A'B' + A'B) + ABC$



Circuit for the following function.

4

Ans to the Q. No 2

(a)

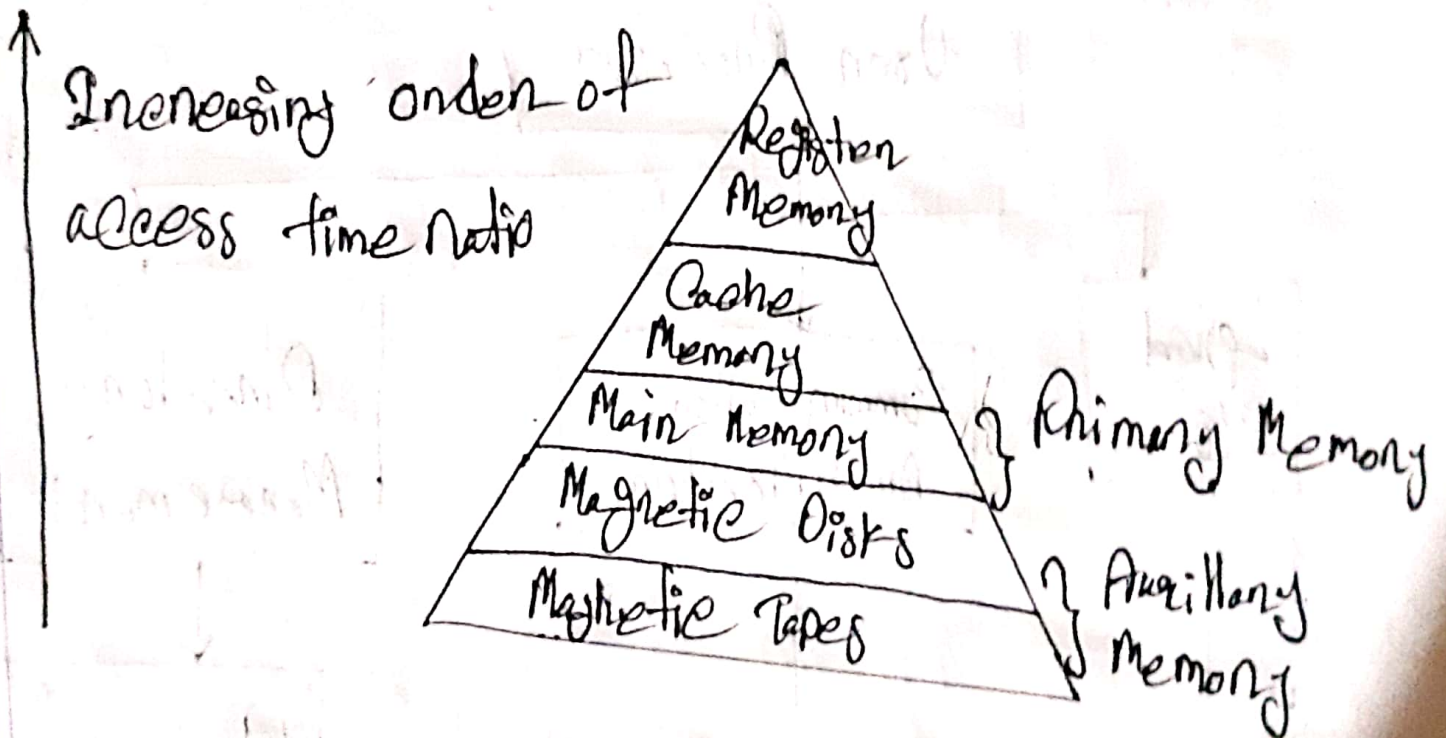
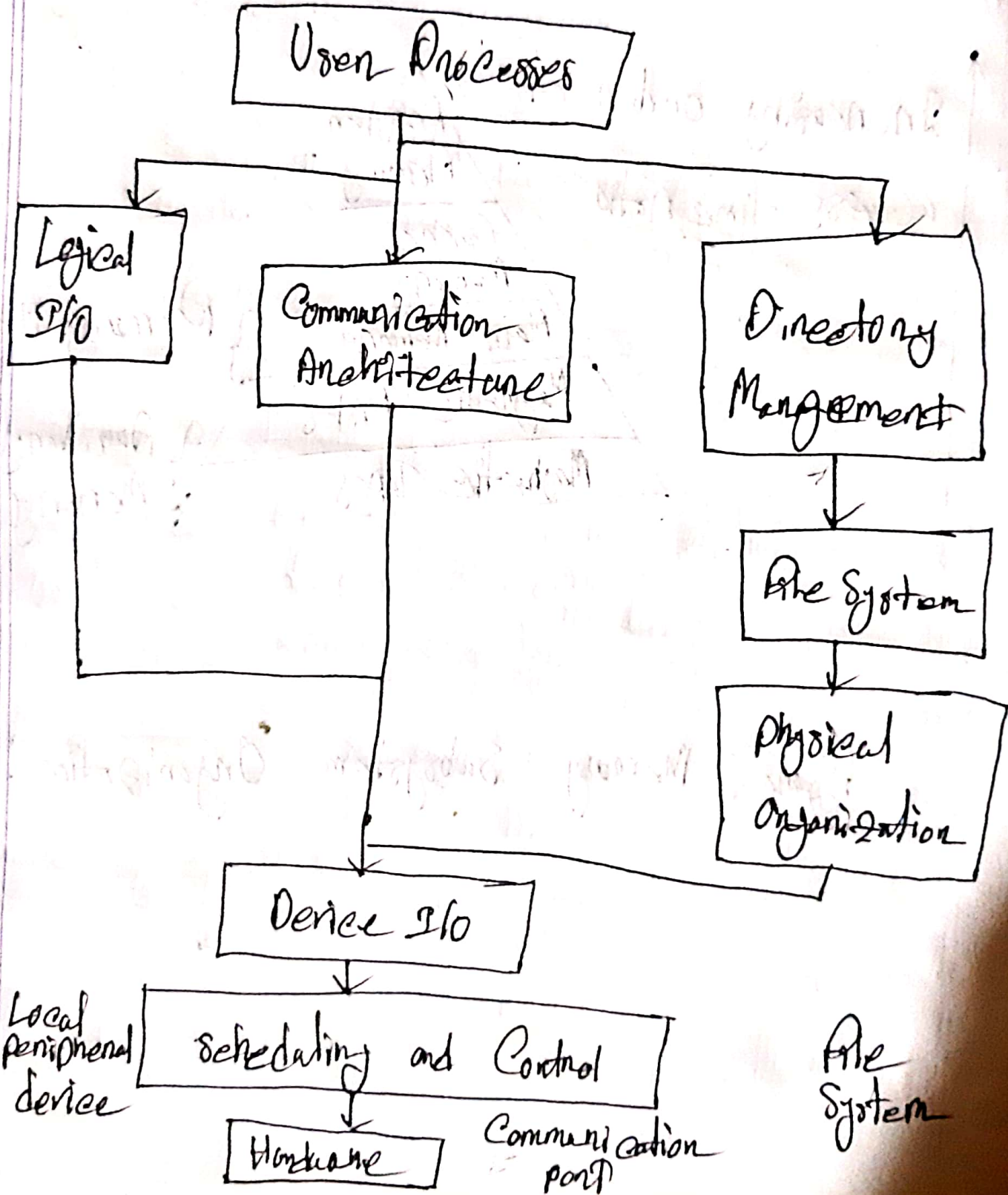


Figure: Memory Subsystem Organization.

Ans to the Q No 3

(a)



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In the model of I/O Subsystem Organization User Processes is the main workstation. Then there are different parts in the organization system. Then the last part is the hardware part. The I/O subsystem of a computer provides an efficient mode of communication between the central system and the outside environment. It handles the input-output system. System devices connected to computer are called peripheral devices:

Ans. to the Q. No 4

(c)

CAM Hardware Organization;

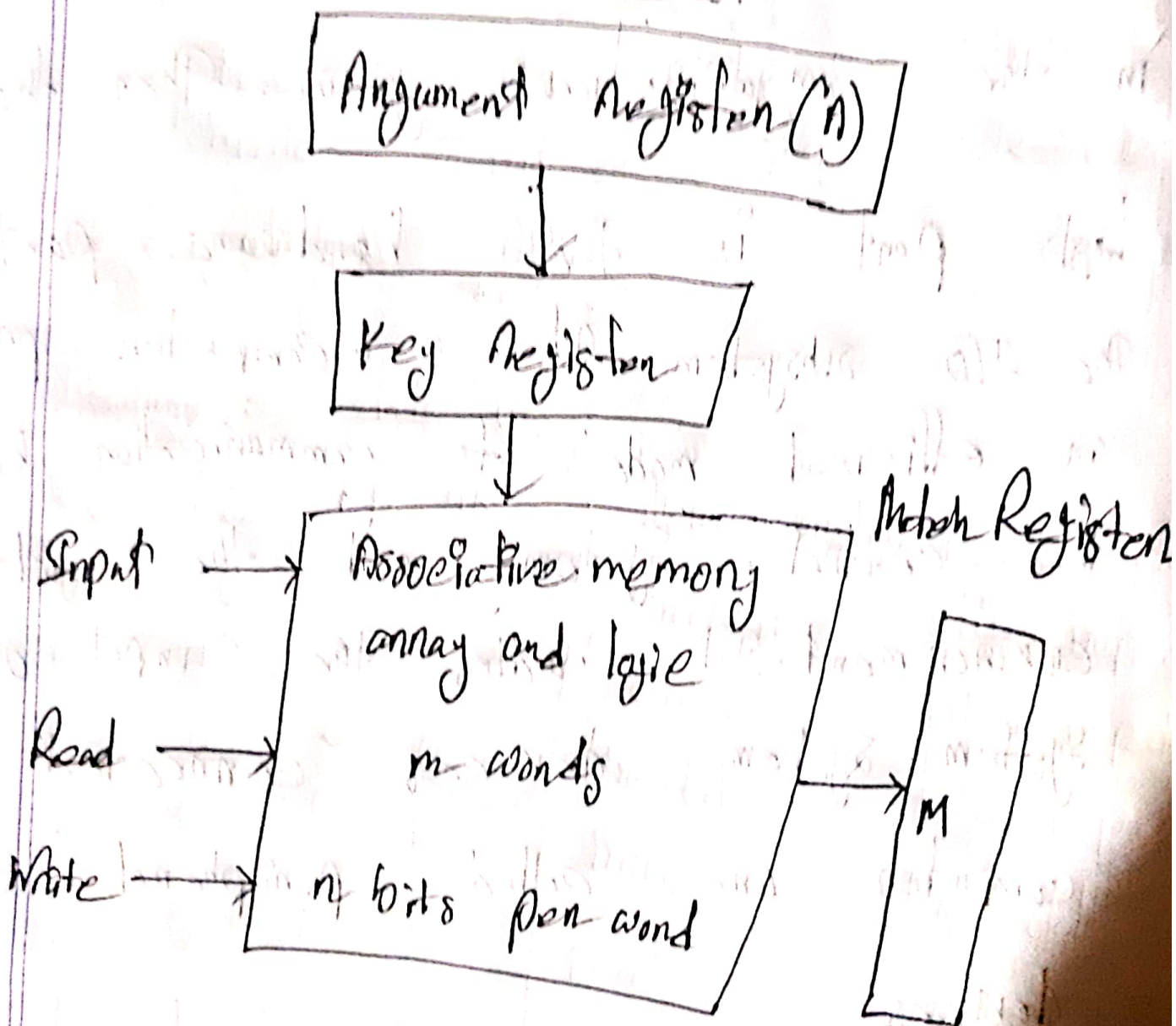


Fig CAM Hardware Organization.

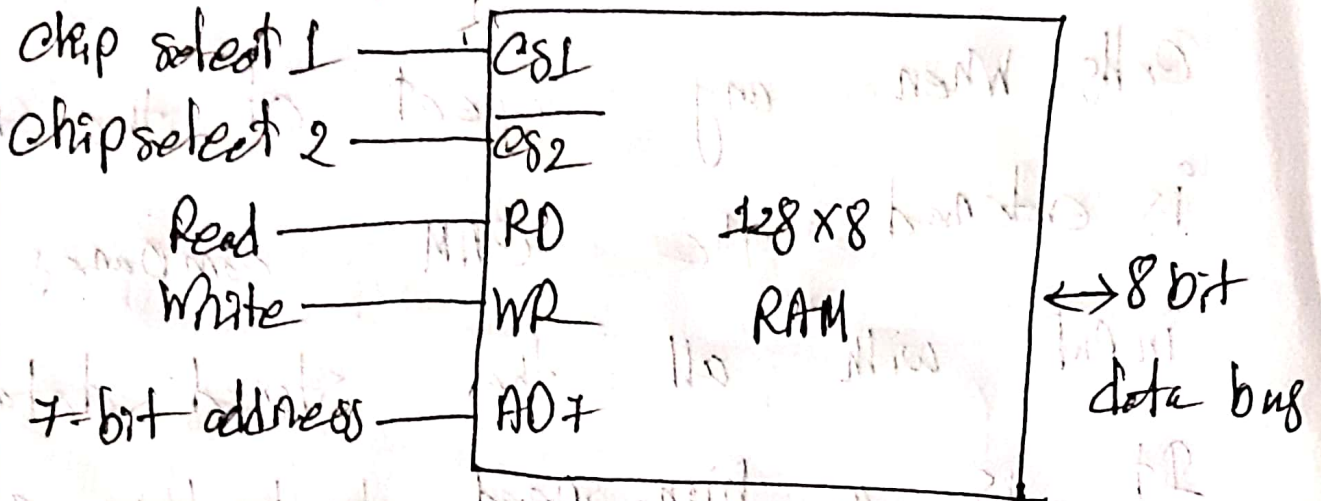
8

Content Addressable Memory is a data storage device, that stores memory in cells. When any aspect of the memory is entered, the CAM compares the input with all the stored data. It is a high-speed technology. In CAM memories are not arranged in chronological order and are not packed in isolated modules.

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Ans-to the Q No. 2 (b)

RAM chip:



Meaning of data bus:

CS1	CS2	RD	WR	Memory function	State of data bus
0	0	x	x	Inhibit	High-impedance
0	1	x	x	Inhibit	High-impedance
1	0	0	0	Inhibit	High-impedance
1	0	0	1	Write	Input data to RAM
1	0	1	x	Read	Output data from RAM
1	1	x	x	Inhibit	High impedance

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The following table is a functional table. It is the meaning of the 8-bit data bus. Functional table means the function the 8-bit data bus.