Victoria University of Bangladesh
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Final Assessment

Ans to the Q's no - 1(b)

When an I/O device completes an I/O operation, the following sequence of hardware events occurs:

(1) The device issues an interrupt signal to the processor.

(2) The processor finishes the execution of the current instruction before responding to the interrupt.

(3) The processor test for an interrupt and sends an acknowledgement signal to the device that issued the interrupt.

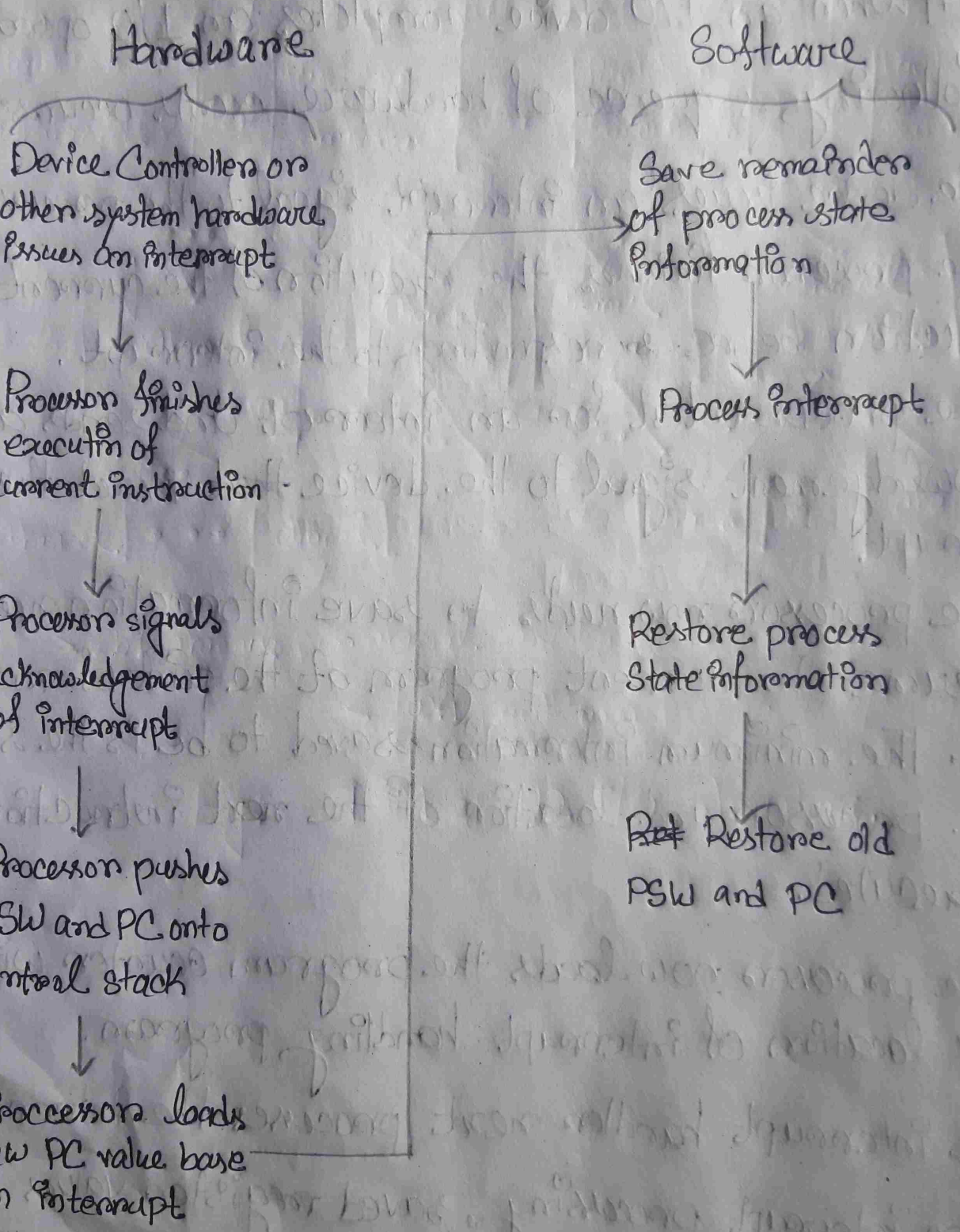
(4) The processor now needs to save information needed to resume the current program at the point of an interrupt. The minimum information saved to be is the status of the processor and location of the next instruction to be executed.

(5) The processor now loads the program counter with the entry location of interrupt handling program.

(6) The interrupt handler next proceses the interrupt.

(7) After interrupt processing, saved register values are

retrieved from stack and restored and next instruction will be executed.



Ans to the Q no - 1(a)

The zEC12 I/O subsystem is similar to the one on ~~z196~~ z196 and includes a PCIe ~~infra~~ infrastructure. The I/O subsystem is supported by both a PCIe bus and an I/O bus similar to that of z196. It includes the infiniband double date rate (IB-DDR) infrastructure, which replaces the self-timed interconnect that was in previous System z systems. This infrastructure is designed to reduce processor usage the latency and provide increased throughput. The I/O expansion network uses the infiniband link layer (IB-2, Double Data Rate).

zEC12 also offerses three I/O infrastructure elements for holding the I/O features: PCIe I/O drawers, for PCIe features; and I/O drawers and I/O cages, for non-PCIe features.

Channel structure:-

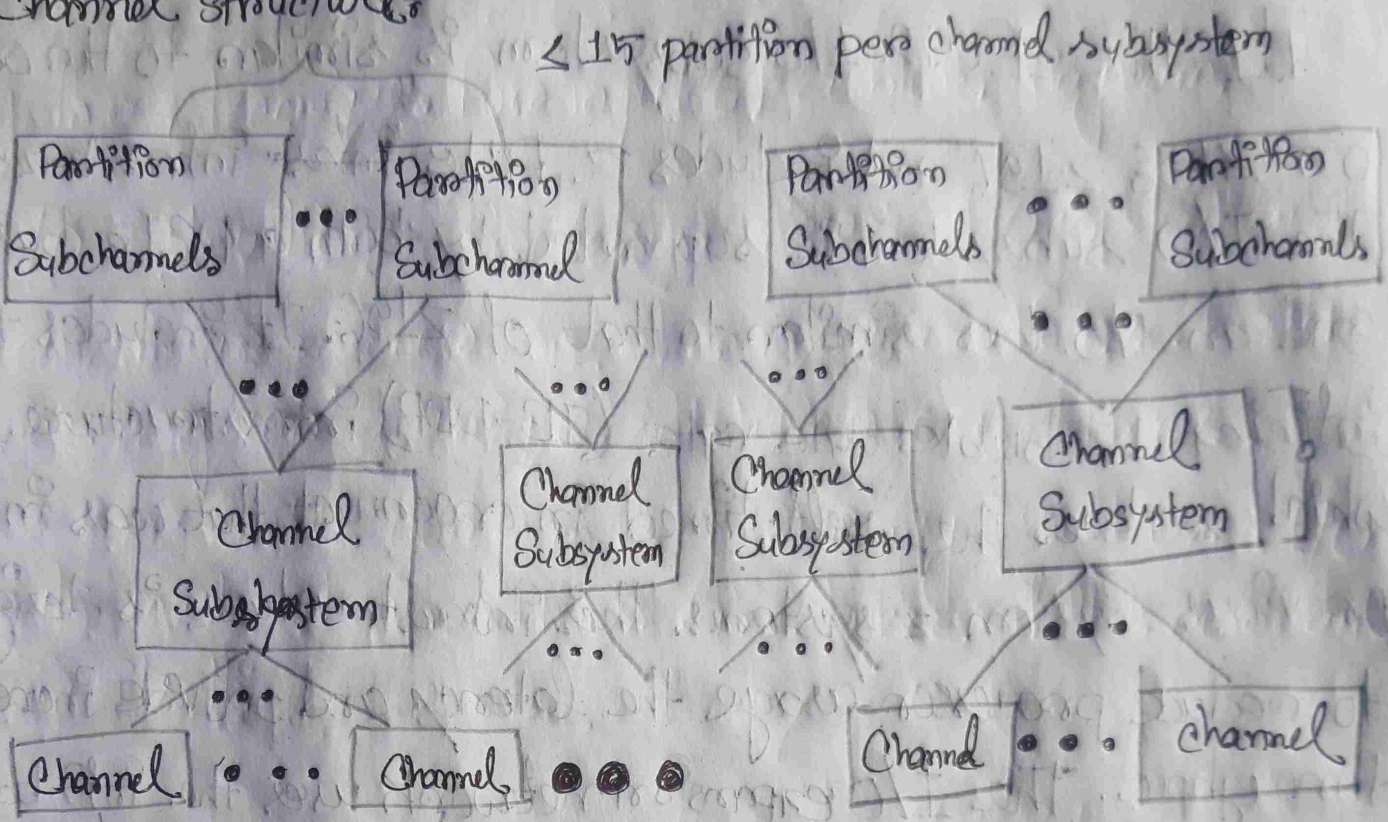


Fig:- IBM zECI2 I/O structure.

Ans to the Q no - 1(c)

Three techniques for input of a block diagram:-

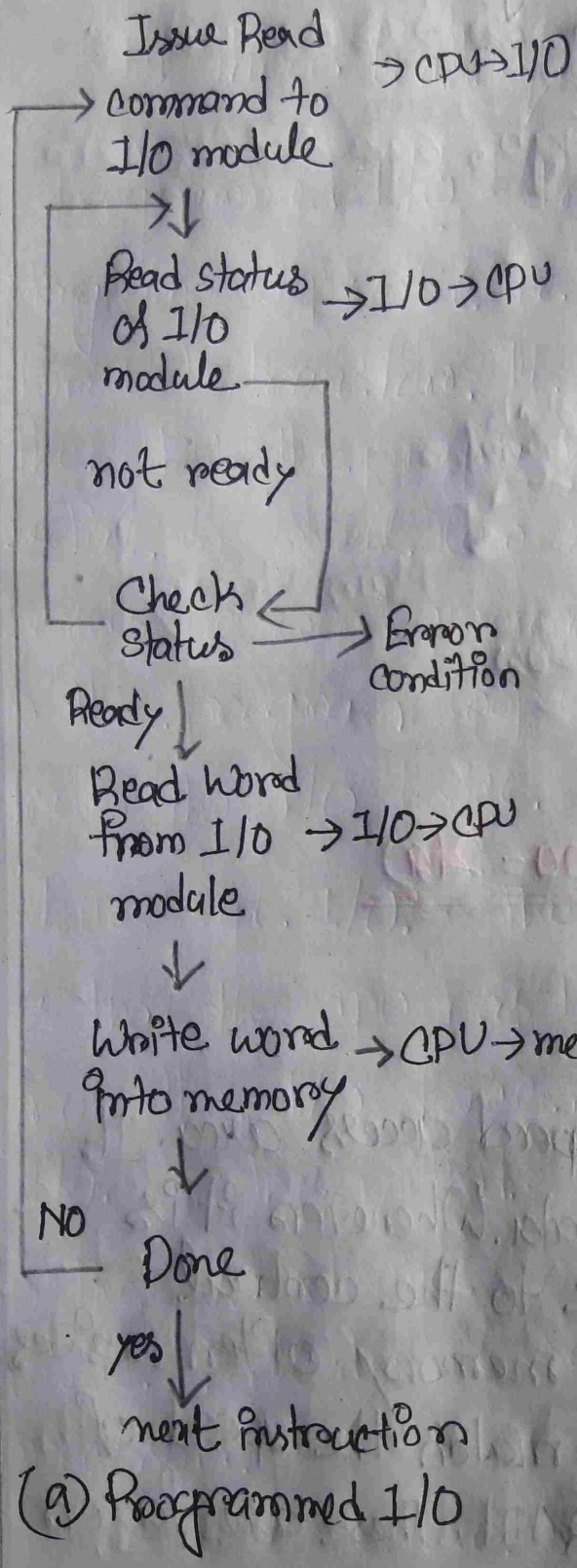
Programmed I/O:- In this method, the CPU stays in a program loop until the I/O unit indicates that is ready for data transfer. It is a time consuming process for the CPU. The programmed I/O method is particularly useful in small low ~~spped~~ speed computers. The CPU sends the 'read' command to the I/O device and waits in the program loop until it receives a response from the I/O device.

Interrupt I/O:- The problem with Programmed I/O is that the CPU has to wait for the ready signal from the I/O device. So alternative to this is interrupt I/O. In this method, the CPU issues a read command to the I/O device about the status. When the I/O device is ready it sends an interrupt signal to the processor.

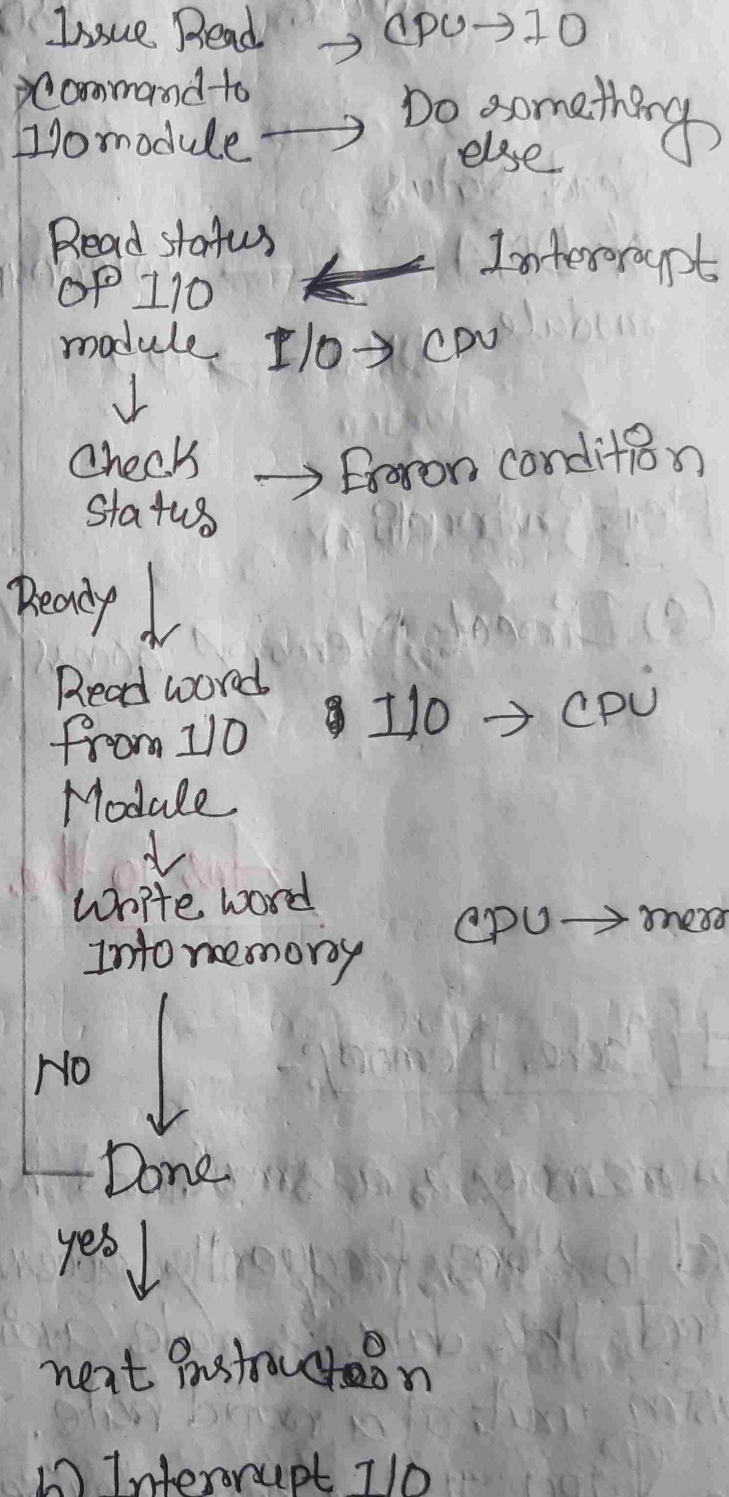
When CPU recieves the signal from the device, it checks the status. If the status is ready, then the

CPU read the word from the I/O device and writes the word in the main memory. If it's done successfully, then the processor will go to the next instruction.

Direct Access Memory (DMA):- Letting the DMA controller (DMAC) ~~manages this process~~ is to manage the memory buses directly. It would improve the speed of data transfer. A chip says a DMA controller (DMAC) manages this proces. The CPU is idle and it has no control over the memory buses. A DMA controller takes over the buses to manage the transfer directly between the I/O device and memory.



(a) Programmed I/O



(b) Interrupt I/O

Issues Read block command to I/O module → CPU → DMA → Do something else

Read status of DMA module ← Interrupt DMA → CPU

↓

Next instruction

(c) Direct Memory access.

Ans to the Q no - 2(a)

Cache Memory:-

Caches memory is a small and high speed access area. It is used to store frequently accessed data. Whenever it is required, this data is made available to the central processing unit at a rapid rate. This memory often resides in the CPU. It has been devised to match the speed of the processors, it is Static-RAM, SRAM. These are faster

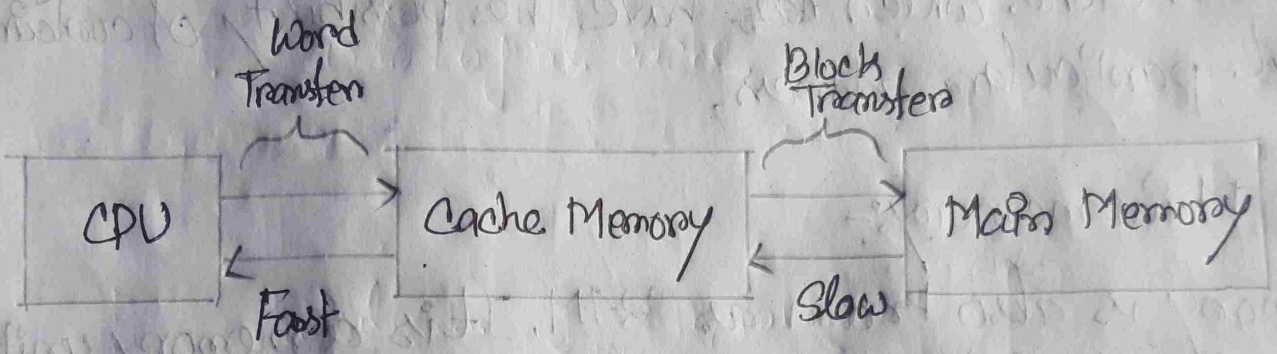
Ca and expensive than DRAM.

Cache memory is located between main memory and CPU. If a processor needs to write or read a ~~loc~~ location in the main memory, it checks the availability of the memory location in the cache. Its done by comparing the address of the memory location to all the tags in the cache which ~~has~~ have the possibility of containing that particular address.

Main memory:-

Memory is also known as RAM. It is a memory unit that directly interacts with the CPU. It is a volatile source of data. It can be described as a large array comprising of words or bytes. RAM is connected with the processor by its address and data buses. This buses are composed as electrical circuits or bits. Main memory is actually built ~~fo~~ from DRAM chips or Dynamic RAM. They are known for their compact size and capability for a faster access. It is important to mention that the computers can only manipulate data that is present in the main memory. ~~It~~ A typical "module" of desktop

memory is long and thin in appearance. It is installed in the memory module slots present on the motherboard. Moder memory modules come in various capacities like 256mb, 512mb, 1gb, 2gb, 4gb, 8gb sizes; main memory has a limited capacity.



Ans to the Q no- 2(b)

Logical cache:-

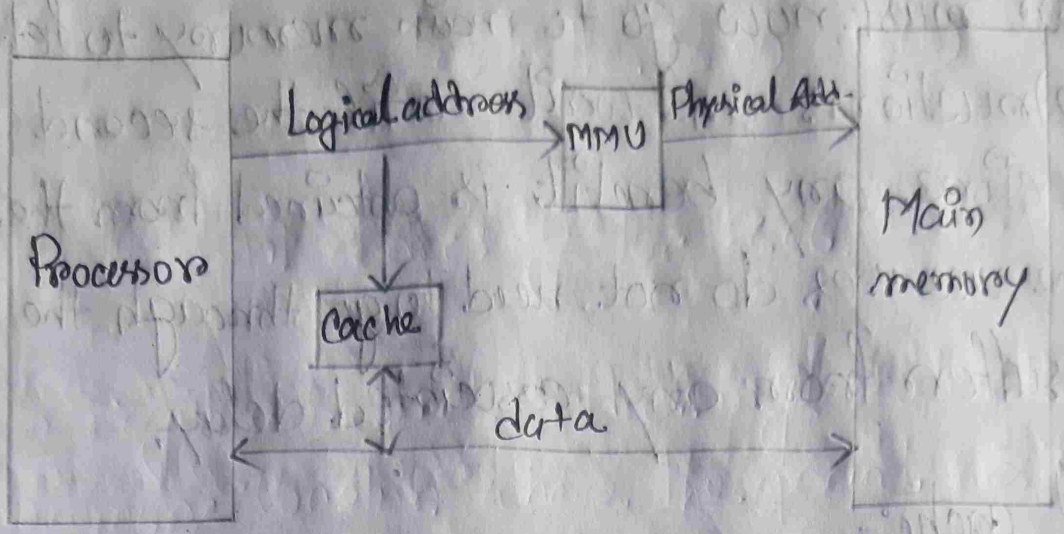
With a logical cache the tag information refers to the logical addresses currently in use by the executing task. If the task is switched out during a context switch, the cache tags are no longer valid and the cache, together with its often hard-won data must be flushed and cleared.

The processor must now go to main memory to fetch the first instructions and wait until the second interaction before any benefit is obtained from the cache. However, cache accesses do not need to go through the MMU and do not suffer from any associated delay.

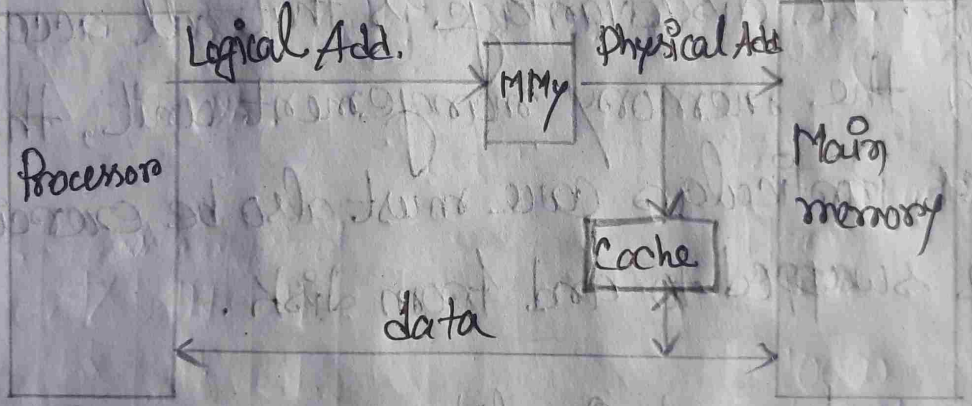
Physical Cache:-

Physical cache use physical addresses, do not need flushing on a context switch and therefore data is preserved within the cache. The disadvantage is that all accesses must go through the memory mangement unit, thus incurring delays. Particular care must also be exercised when pages are swapped to and from disk.

If the processor does not invalidate any associated cache entries, the cache contents will be different from the main memory contents by virtue of the new page that has been swapped in.



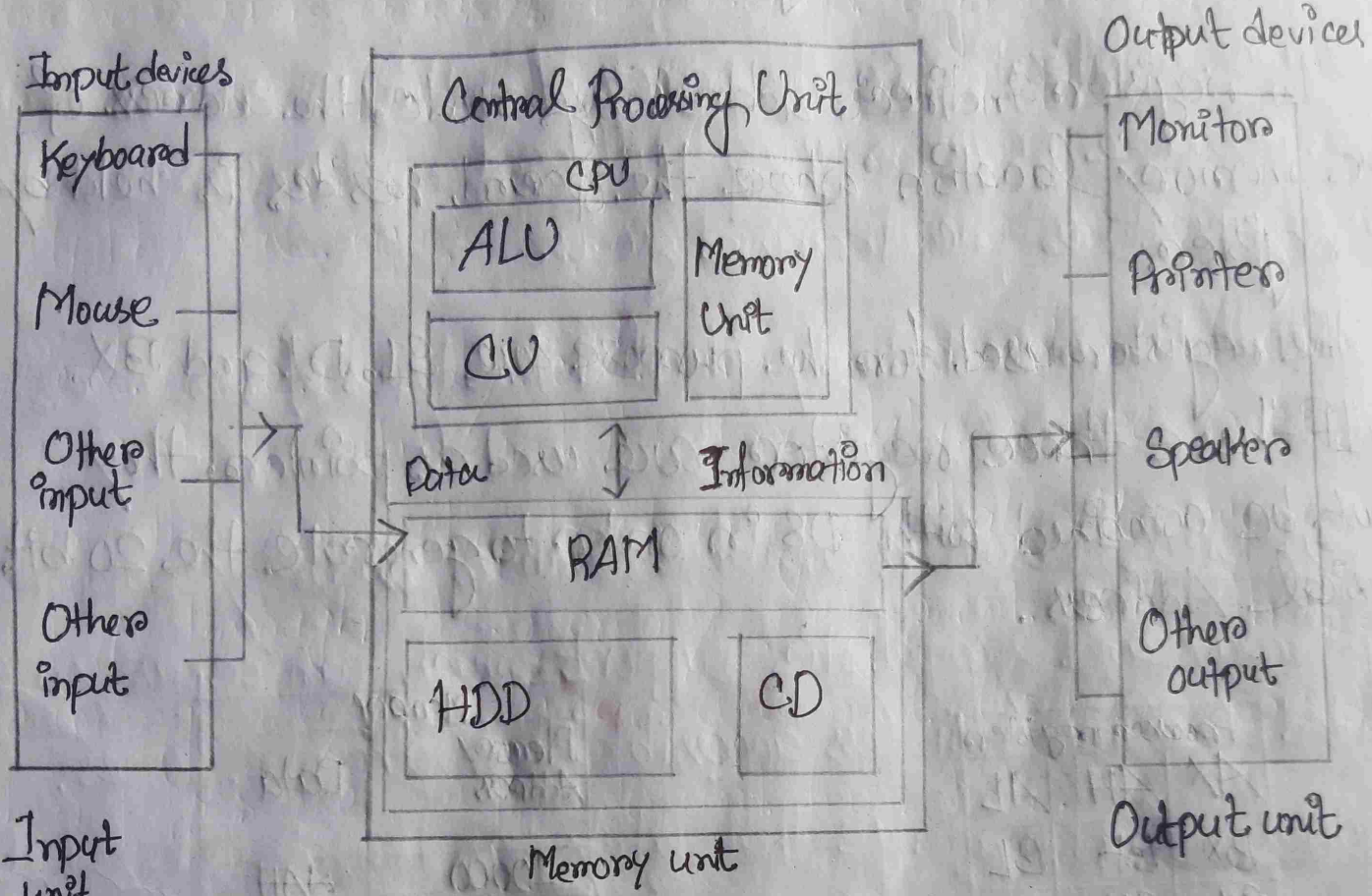
a) Logical cache



b) Physical cache.

Ans to the Q no - 3(a)

Computer system:-



Central processing unit:-

Central Unit:- ALU, CU, Memory unit.

Memory unit:- ~~RAM~~, HDD, CD

Ans to the Q.no - 3(b)

Indirect addressing for x86:-

In register indirect addressing mode, the address of the memory location where the operand resides is held by a register.

The registers used for the purpose are SI, DI and BX.

If these three register are used as pointers, they must be combined with DS in order to generate the 20 bit physical Address.

Processor registers		
AX	AH	AL
BX	BH	BL
CX	CH	CL
DX	DH	DL
SI		
DI		
BP		
SP		
CS		
DS		
SS		
ES		

Memory	
Memory Address	Data
10000	AAH
10001	BBH
10002	CCH
10003	EEH
10004	DDH
10005	EEH
10006	FFH
10007	11H
10008	22H
10009	33H
1000A	44H