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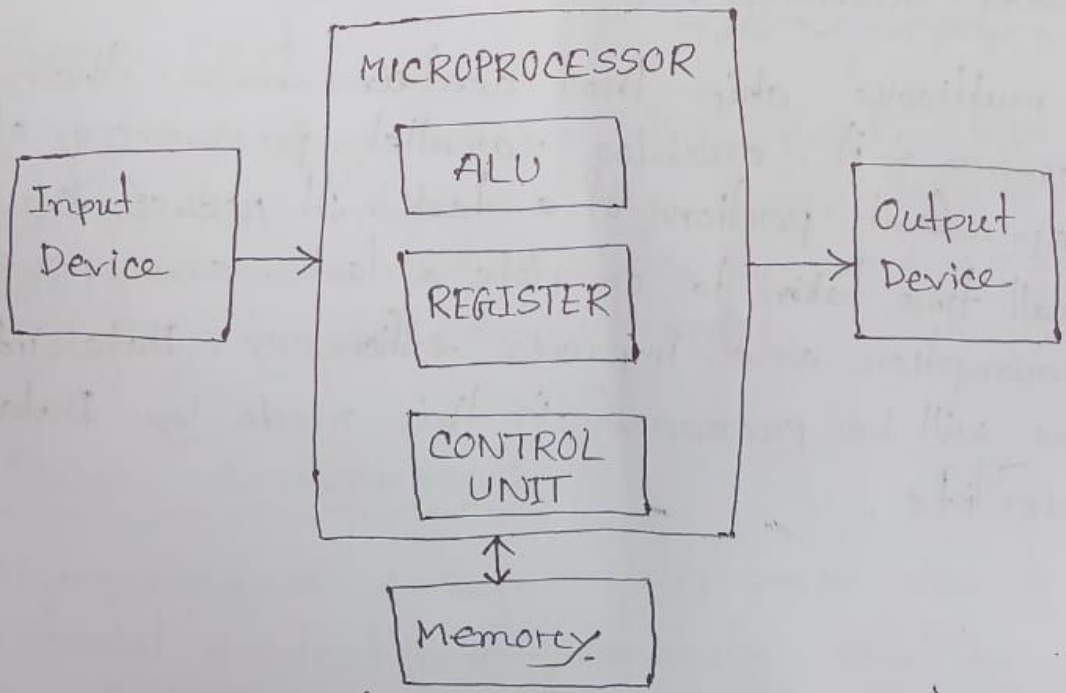
C. Code : CSE - 413

Ans. to the Q. No - 01

(a)

Microcomputer :-

A digital computer with one micro-processor which acts as a CPU is called microcomputer. Computer's Central Processing Unit (CPU) build on a single Integrated Circuit is called microprocessor.



Blog Diagram of Basic Microcomputer

Features of Microprocessors :-

Features of Microprocessors are given below :-

1. Architecture :-

Microprocessors are available in 8 bit, 16 bit, 32 bit, 64 bit architectures. This bit size indicates the size of the data, the processor can handle and the scope of the memory the processor can address during its operation. The bit sizes can also be called bus width.

As the processor width increases program code size comes down. Though it largely challenging to code in 64 bit processor than 8 bit, the external tool, aides, Integrated development environment make it easier to develop programs in computers with higher width processor. Due to this labour cost also is lower.

2. Parallel Processing :-

The multicore chip that contains more than one processor in it, enables parallel processing of independent portions of a task. It reduces the overall time taken to complete a task, saves power consumption and improves efficiency. Data-intensive jobs will be processed in this mode by Data Scientists.

3. Multiprocessing and time sharing :-

The time is divided into several equal slices and it is allotted to various processes in a round-robin fashion. As the available CPU is only one in the system and that CPU will process that allotted process for that slice of time or till the interrupt occurs whichever is earlier, The computer resource is shared across multiple process running concurrently.

4. Categories of Microprocessors :-

Based in the way instruction set is constructed and how they getting executed, microprocessors are categorised into

a) Reduced Instruction Set Computers (RISC)
b) Complex Instruction Set Computers (CISC)
c) Special Purpose Processors.

5. Size : Cost :-

As the technology improves the cost either comes down or the value for the money increases. The user gets more features for the same money or a slightly higher amount spent.

6. Power Consumption :-

Microprocessors consume less power due to their material content and technology used in manufacturing.

7. Versatility :-

Microprocessors can be deployed for multiple purposes by simply configuring the software in them.

8. Reliability :-

Microprocessors are highly reliable in their operation and their performance is steady even under complex conditions.

(c) Bit manipulation Instruction :-

Bit manipulation instruction sets are extensions to the x86 instruction set architecture for microprocessors from Intel and AMD.
The purpose of these instruction sets is to improve the speed of bit manipulation. All the instructions in these sets are non-SIMD and operate only on general-purpose registers.
There are two sets published by Intel : BMI and BMI2; They were both introduced with the Haswell microarchitecture with BMI1 matching features offered by AMD's ABM instruction set and BMI2 extending them. Another two sets were published by AMD: ABM and TBM.

Bit manipulation is the act of algorithmically manipulating bits or other pieces of data shorter than a word. Computer programming tasks that require bit manipulation include low-level device control, error detection and correction algorithms, data compression, encryption algorithms and optimization. For more other tasks, modern programming languages allow the programmer to work directly with abstractions instead of bits that represents those abstractions. Source code that does bit manipulation makes use of the bitwise operations: AND, OR, XOR, NOT, and possibly other operations analogous to the boolean operators; there are also bit shifts and operations to count ones and zeros, find high and low one or zero, set, reset and test bits, extract and insert fields, mask and zero fields, gather and scatter bits to and from specified bit positions or fields.

Bit manipulation, in some cases, can obviate or reduce the need to loop over a data structure and can give many-fold speed ups, as bit manipulations are processed in parallel.

1/(b):

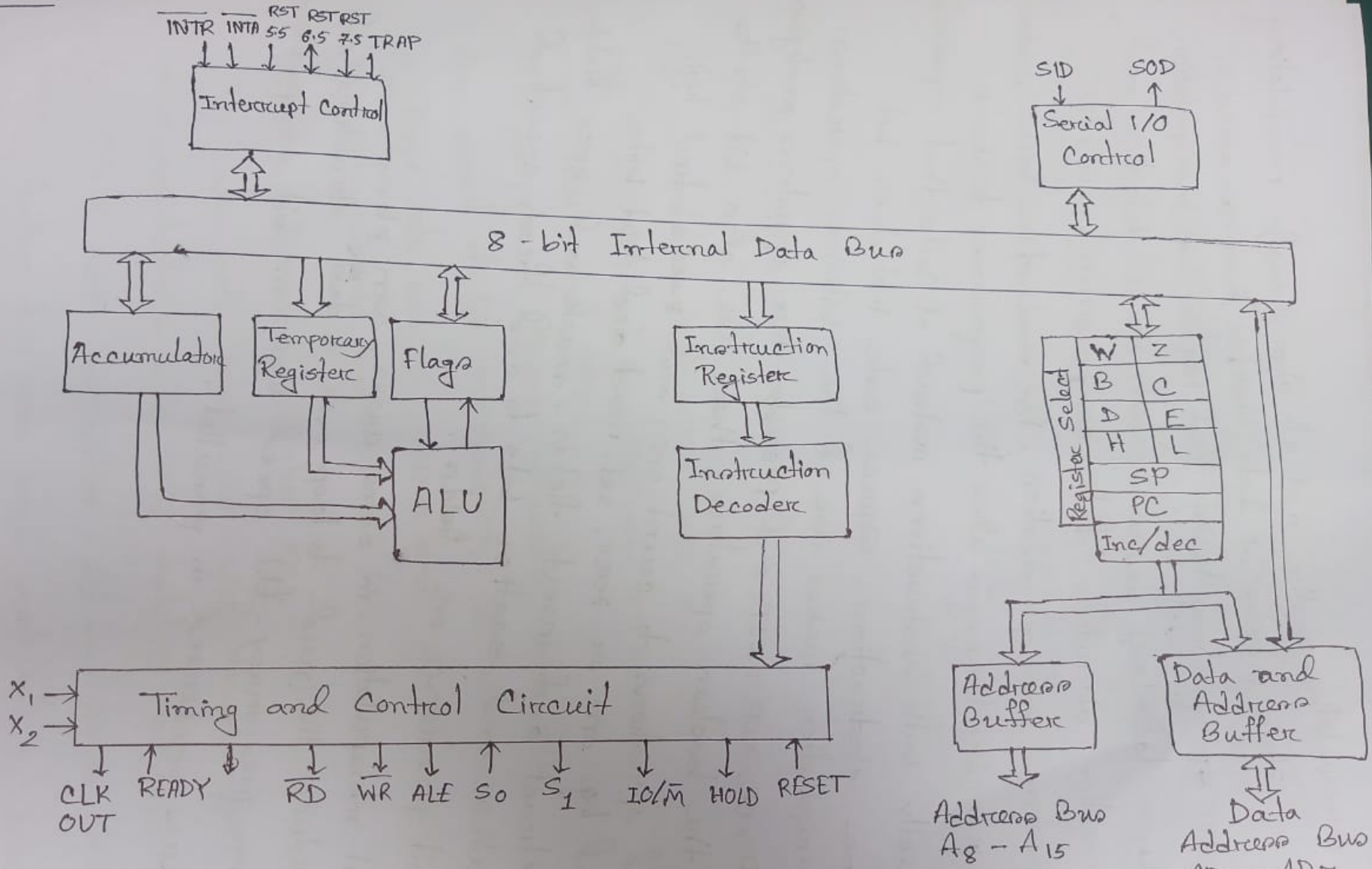


Fig: Architecture of 8085 Microprocessor

Ans. to the Q. No – 02

(a) How DMA Operations are performed :-

Initially, when any device has to send data between the device and the memory, the device has to send DMA request (DRQ) to DMA controller.
The DMA controller sends Hold request to the CPU and waits for the CPU to assert the HLDA.

(b) 8257 pin discription :-

40-pin DIP

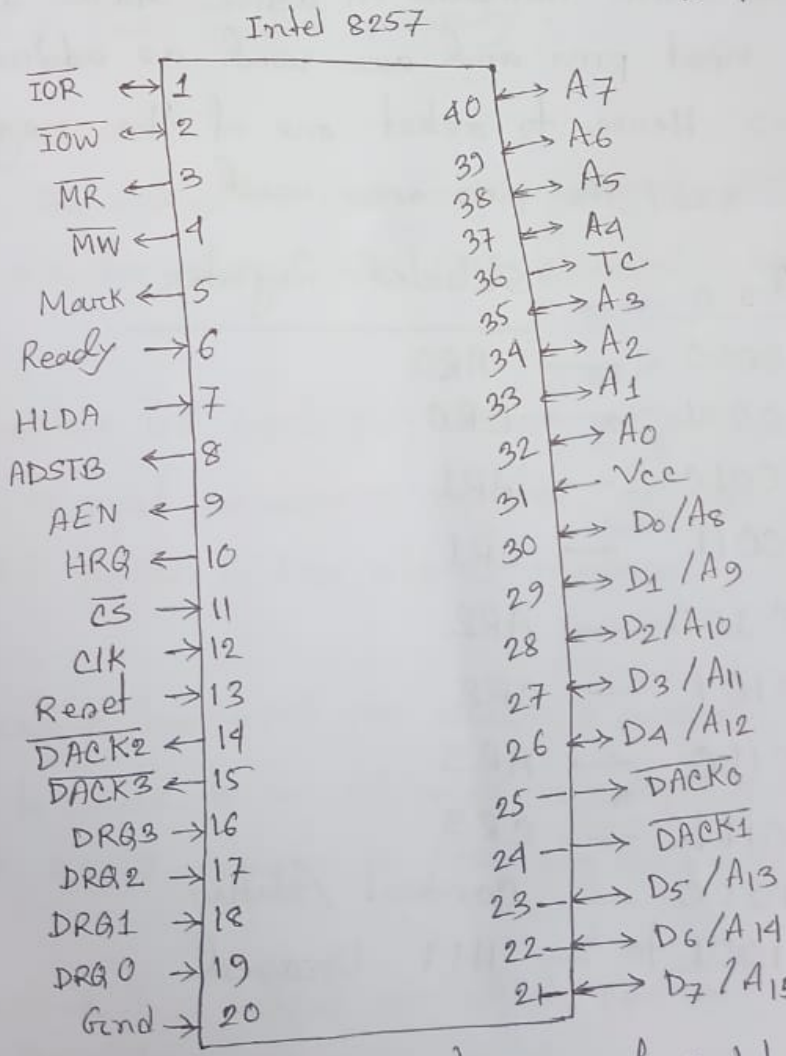


Fig : Physical pin diagram of Intel 8257

Discription :-

D_7-D_0 / A_{15-8} :

For communicating with the processor there are 8 bidirectional data pins, when the processor is in active and the 8257 active state it is in slave mode. When the processor remains in the HOLD state and 8257 behaves as the masters, they are used to send out the most significat 8 bits of memory address.

A_{3-0} :

When the processor remains in active state and are used as address input pins and are used as address input pins of 8257. Hence to select one of the registers inside the 8257 the pins are used.

A_{3-0}		Selected Register
0000	—	AR0
0001	—	CR0
0010	—	AR1
0011	—	CR1
0100	—	AR2
0101	—	CR2
0110	—	AR3
0111	—	CR3
1000	—	Control / Status
1001 to	—	1111 Unused

RESET :-

RESET is an active high input pin which is connected to the reset outpin of 8085. After 8257 is reset, the control register contents turn to 00H.

DRQ 3-0 :

These pins are active high DMA request input pins, assigned to one for each DMA channel. These are activated by some special-purpose I/O port chips like Intel 8257 floppy disk controller, and Intel 8275 CRT controller. In fixed priority mode DRQ0 has the highest and DRQ 3 the lowest priority.

DACK 3 -0* :

These are the active low DMA acknowledged output pins, only for one for every four DMA channels, Intel 8275.

IOR* :

It is an active low input pin which is activated by the processor to read an address register, counter register when 8257 works in the slave mode.

IOW* :

It is an active low input pin which is activated by the processor to write to an Address register, counter register when the 8257 remains in the slave mode,

MR* :

It is an active low output pin which operates tristate when 8257 is in the slave mode.

MW*: It is also an active low output pin which is in tristate when 8257 is in the slave mode.

CS*: Unlike others it is also an active low input pin for selecting chip.

CLK: It is the input pin of the clock. The maximum allowed frequency for this clock is about 3 MHz. The input of the clock is connected to the output of 8085 in a system which is based on 8085.

Ready: Ready is an active high input pin which has similar function like the ready input of 8085.

HRQ: HRQ is for HOLD request which is an active high output pin also connected to the HOLD input of 8085.

HLDA: HLDA means HOLD acknowledge which is an active high input pin, that is connected to the HLDA output of 8085.

TC: TC means terminal count which is an active high output pin.

MARK: This is also an active high output pin which is activated when the least significant 7 bits of the control register become 0 for the DMA channel which is getting serviced.

AEN: AEN stands for address enable. It is an active high output pin performing the same function to output of 8085.

ADSTB: ADSTB signifies address strobe which is an active high output pin performing the same function to output of 8085. In intel 8257, if there is output on this pin as 0, it is in the slave mode.

Ans. to the Q. No - 03

(a)

Rotate Instructions:-

The following instructions come under this category :

Instruction	Description
RCL	Rotate all bits of the operand left by specified number of bits through carry flag.
RCR	Rotate all bits of the operand right by specified number of bits through carry flags
ROL	Rotate all bits of the operand left by specified number of bits.
ROR	Rotate all bits of the operand right by specified number of bits.

Shift instructions :-

The following Instructions come ~~from~~ under this category :-

Instructions	Descriptions
SAL or SHL	Shifts each bit of operand left by specified number of bits and put zero in LSB position.

Instruction	Description
SAR	Shift each bit of any operand right by specified number of bits. Copy old MSB into new MSB.
SHR	Shift each bit of operand right by specified number of bits and put zero in MSB position..

Branch Instruction :-

The following Instructions come under this category:

Instruction	Description
JA or JNBE	Jump if above, not below or equal i.e; when cf and ZF = 0
JAE/JNAE/ JE JNC	Jump if above, not below, equal or carry i.e; when cf = 0
JB/JNAE/JC	Jump if below, not above, equal or carry i.e; when cf = 0
JBE / JNA	Jump if below, not above or equal i.e, when cf and ZF = 1
JCXZ	Jump if cx register = 0
JE / JNL JZ	Jump if zero or equal, i.e. when ZF = 1

Instruction	Description
JG/JNLE	Jump if greater, not less or equal. i.e, when ZF=0, CF=OF
JGE/JNL	Jump if greater, not less or equal. i.e, when SF=OF
JL/JNGE	Jump if less, not greater than or equal. i.e when SF≠OF
JLE/JNG	Jump if less, equal or not greater. ie when ZF=1 and SF≠OF
JMP	Causes the program execution to jump unconditionally to the memory address or label given in the instruction.
CALL	Calls a procedure whose address is given in the instruction and saves their return address to the stack.
RET	Returns program execution from a procedure to the next instruction or main program.
INT	Used to generate software interrupt at the desired point in a program.
INTO	Software interrupts to indicate over flow after arithmetic operation.
LOOP	Jump to defined label until cx=0.
LOOPNZ/ LOOPE	Decrement cx register and jump if cx≠0 and ZF=1
LOOPNZ/ LOOPNE	Decrement cx register and jump if cx≠0 and ZF=0.

Here, CF = Carry Flag.
ZF = Zero Flag
OF = Overflow Flag
SF = Sign Flag
CX = Register

(b) Memory Interfacing :-

When we are executing any instruction, the address of memory location or an I/O device is sent out by the microprocessor. The co-responding memory chip or I/O device is selected by a decoding circuit. Memory required some signal to read from and write to registers and microprocessor transmits some signals for reading and/or writing data. The interfacing process includes matching the memory requirements with the microprocessors signals.

I/O Interface :-

As we know, Keyboard and displays are used as communication channel with outside world. Therefore, it is necessary that we interface Keyboard and displays with the microprocessor. This is called I/O interfacing for this type of interfacing, we use latches and buffers for interfaing the keyboards and displays with the microprocessor. But the main drawback of this interfacing is the microprocessor can perform only one function.