Victoria University of Bangladesh
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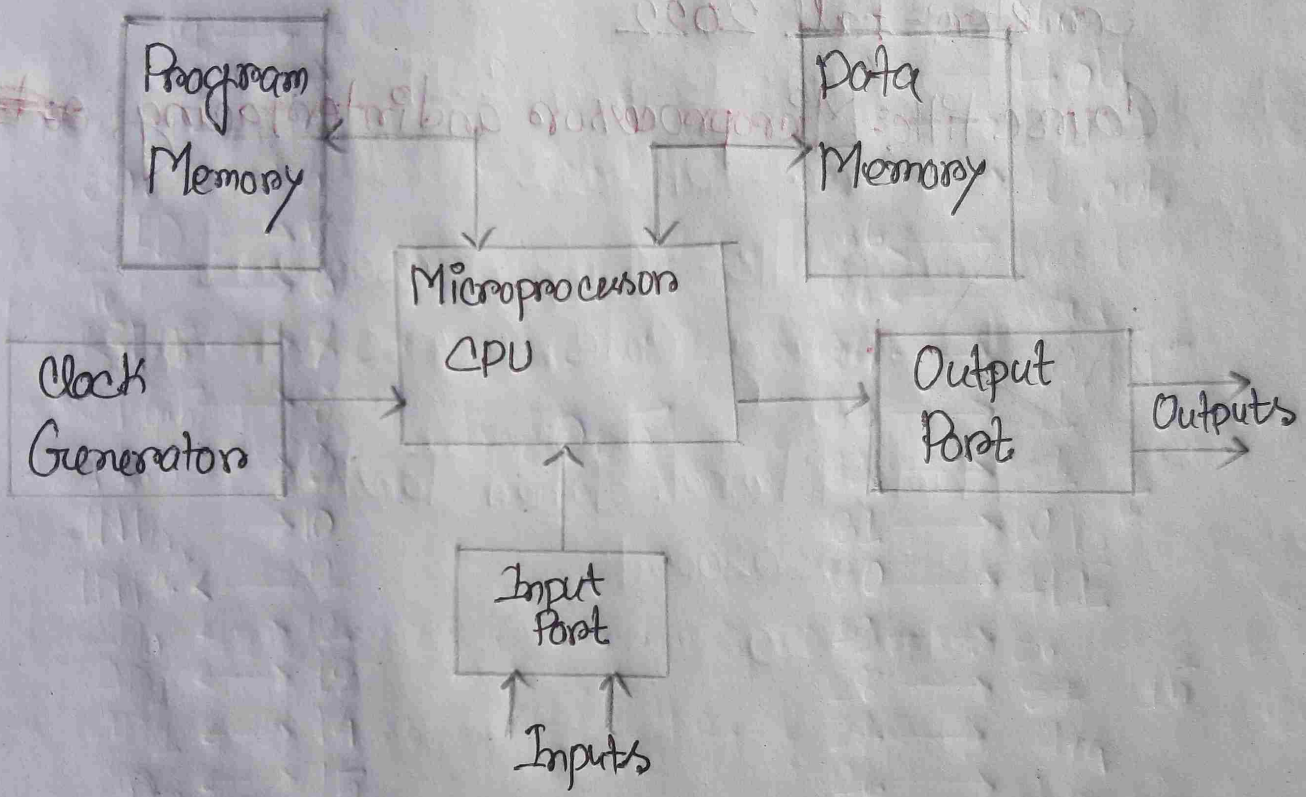
Name:- Nusrat Jahan Tanshee
ID:- 2520200011
Batch:- 20

Final Assessment

Ans to the 8 no - (1) (a)

Block diagram of a basic Microcomputer:-



Features of Microcomputer:-

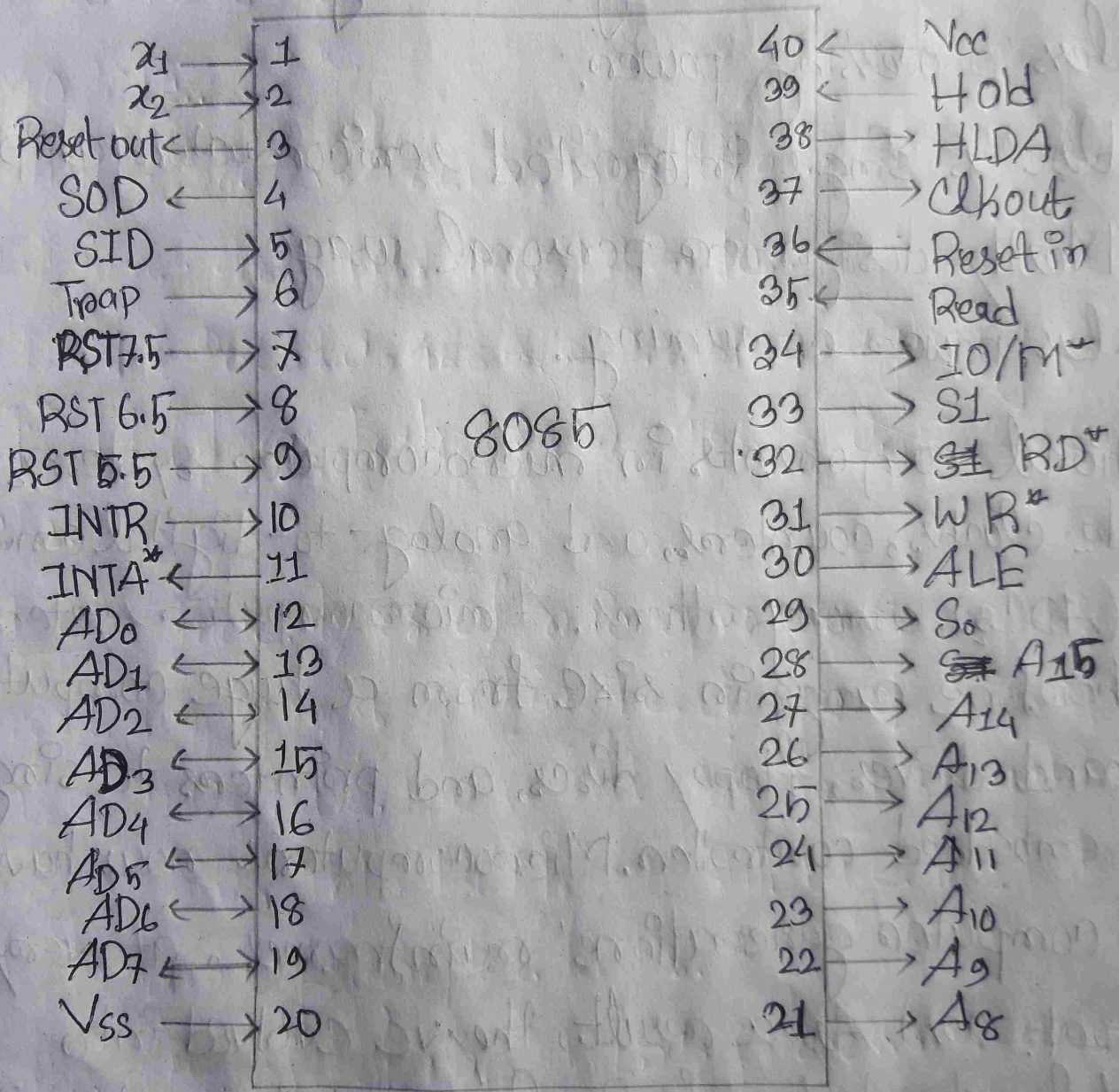
(1) It is small in size
(2) Affordable cost
(3) Different software can be run on the microcomputer.

④ Using by a ~~Sme~~ single user.
⑤ Mostly microcomputer are portable.
⑥ Produce less heat.
⑦ No need well training for using it.
⑧ less processing power.
⑨ Use a single integrated semiconductor chip.
⑩ Mostly design for personal usage.
⑪ less power consuming.

Additional components in microcomputer systems include clocks, counters, and analog-to-digital converters (ADCs), among others. A microcomputer system can therefore range in size from a huge computer with hard drives, floppy discs, and printers to single chip embedded controllers. Microcomputers now have more computer generations' mainframes, at very low ~~cost~~ cost. As a result, they've evolved into powerful networked professional ~~workstat~~ workstations for corporate uses.

Ans to the Q no - (1) (b)

Draw 8085 pin configuration:-



Intel 8085 is fabricated as a 40 pin DIP-IC. DIP stands for "dual inline package". It means the package will have pins on only 2 sides, 20 on each side in this case.

Ans to the Q no-(1)(c)

(4) Define classification of Microprocessor:-

In general, there are mainly 3 types of processor which is as follows:-

(i) CISC - complex instruction set computers
(ii) RISC - reduced instruction set computers, and
(iii) Special purpase processors

CISC:- These types of microprocessors are microcode ~~operade~~ operated. Microcode could be a set of instructions (software) for microprocessor that run invisibly inside the chip.

The listing of popular CISC processors is shown below.

(viii) Intel - 8085, 8088, 8086, 80286, 80386SX, 80386DX, 80486SX, 80486DX, Pentium, dual core, quard core etc.

(v) Motorola - 6800, 68000, 68010, 68020, 68030, 68040 etc.

(vi) AMD - 386DX, 486DX, K5, Athol, 64x2 dual core.

(vii) Cyrix - 486DLC, 486SLC2, etc.

(ix) IBM - 386SLC, 486SLC2, Blue lighting

(x) TI (Texas Instrument) - 486 SLC/E, 486 DLC/E. etc.

RISC:- These types of microprocessors represent a recent development within the design of microprocessors. RISC CPUs have fewer and simpler instructions programmed into ROM, yet still have the potential of performing complex tasks.

The list of popular RISC processors are -

(v) DEC Alpha: 21064, 21064A, 21068 etc.

(i) SPARC: TMS 390S10

(ii) IBM, Apple and Motorola Power PC: 601, 604, 603, 620 etc.

(iii) MIPs - R10000.

Special Purpose Microprocessor:-

These types of microprocessors are used for specific applications or to boost the performance of main processor. A ~~Co-~~ coprocessor can be said as an example of the special purpose processor. Most micro~~pro~~ computers support the employment of one or more coprocessors.

Example: Intel 8087, 80287, 80387, 487 etc. Cyrix 83DS7, EMC87; Weitek 1167, 3167, 4167 etc.

Ans to the Q no - 2(a)

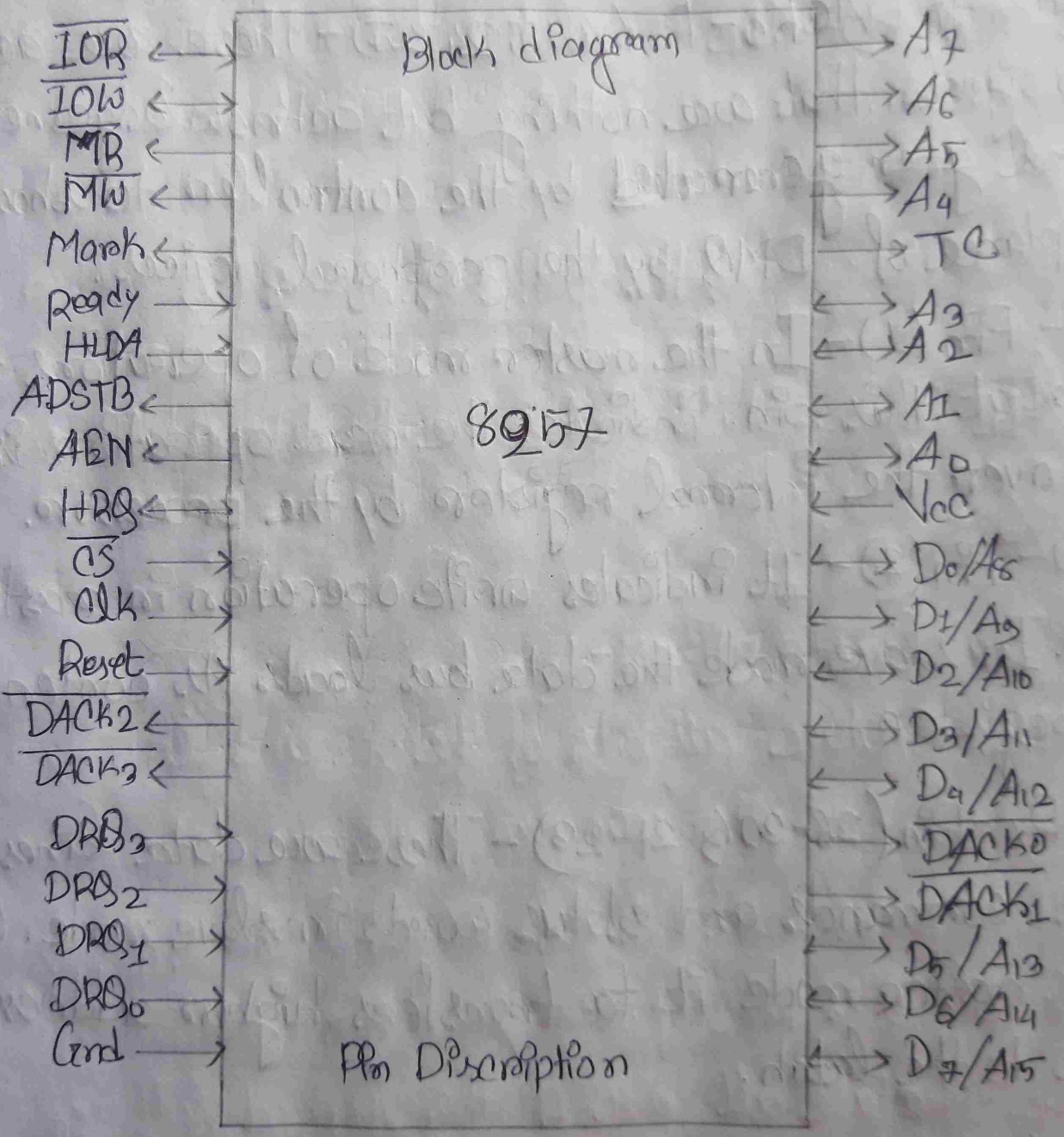
(v) How DMA operations are performed:-

- Initially, when any device has to send data between the device and the memory, the device has to send DMA request (DRQ) to DMA controller.
- The DMA controller sends hold request (HRQ) to the CPU and waits for the CPU to assert the HLDA.
- Then the microprocessor tri-states all the data bus, address bus and control bus. The CPU leaves the control over the bus and acknowledge the HOLD request through HLDA signals.
- Now the CPU is in HOLD state and the DMA controller has to manage the operations over buses between the CPU, memory and I/O devices.

(9)

Ans to the Q no - 2(b)

① Description of the pins in 8257:



DRQ_0 to DRQ_3 - Pin (16-19) - This pins get enabled whenever the input device requests the DMA controller for direct data transfer to the main memory.

$DACK_0$ to $DACK_3$ - Pin (14, 15, 24, 25) - These are active low signals that are nothing but acknowledgement signal ~~gen~~ generated by the controller to show the acceptance of DMQ by the peripheral devices.

IOR - Pin (1) - In the master mode of operations the low signal at this pin indicates the read operation is performed over the internal registers by the processors.

IOW - Pin (2) - It indicates write operation in masters mode. In slave mode the data bus loads its content at the register.

D_0 to D_7 - Pin (26-30 & 21-23) - These are data lines that holds commands and status words in slave mode. While in the master mode it ~~to~~ transfers higher addresses bytes to the latch.

A_0 to A_3 - Pin (32-35) - These are ~~fr~~ 4 least significant address lines that act as input and output in slave and masters operating mode of the system respectively.

A_4 to A_7 - Pin (37-40) - These are basically lower order address lines produced by the controller in master mode.

CLK - Pin (12) - This pin is used to provide an internal clock frequency signal to 8257.

CS - Pin (11) - CS denotes chip and it is an active low pin.

HRQ - Pin (10) - The enabling of this pin shows the request to directly access the memory by the peripheral device for read-write operation.

HLDA - Pin (7) - The enabling of this pin represents the acknowledgement by the processor in response to the HOLD signal of the DMA controller.

MEMR - Pin (3) - A low signal at this particular pin represents that read operations is performing over the memory by the peripheral device.

MEMW - Pin (4) - A low active pin that gets enabled at the time of memory write operation by the peripheral device.

ADSTB - Pin (8) - It stands for address strobe. Enabling this pin will demultiplex the address and data bus using latches.

Vcc - Pin (31) - The signal for the operation is applied at this pin.

Ans to the Q no - 3(a)

[1] Rotate, Shift and Branch instruction set of 8086:-

(i) Rotate instructions:-

RCL - Rotate all bits of the operand left by specified number of bits through carry flag.

RCR - Rotate all bits of the operand right by specified number of bits through carry flag.

ROL - Rotate all bits of the operand left by specified number of bits.

ROR - Rotate all bits of the operand right by specified number of bits.

(3) Shift instructions:-

SAL or SHL - Shifts each bit of operand left by specified numbers of bits and put zero in LSB positions.

SAR - Shift each bit of any operand right by specified number of bits. and Copy old MSB into new MSB.

SHR - Shift each bit of operand right by specified number of bits and put zero in MSB positions.

(4) Branch instructions:-

JA or JNBE - Jump if above, not below, or equal i.e. when CF (Carry flag) and ZF (Zero flag) = 0

JAE/JNB/JNC - Jump if above, not below, equal or no carry i.e. when CF = 0

JB/JNAE/JC - Jump if below, not above, equal or carry i.e. when CF = 0

JBE/JNA - Jump if below, not above, or equal i.e. when CF and ZF = 1

JCXZ - Jump if CX register = 0

JE/JZ - Jump if zero or equal i.e. when ZF = 1

JG/JNLE - Jump if greater, not less or equal i.e. when ZF=0 and CF=OF

JGE/JNL - Jump if greater not less or equal i.e. when SF=OF.

JL/JNGE - Jump if less, equal or not greater i.e. when ~~ZF=1~~ SF≠OF.

JLE/JNG - Jump if less, equal or not greater i.e. when ZF=1 and SF≠OF

JMP - Causes the program execution to jump unconditionally to the memory address or ~~level~~ label given in the instruction.

CALL - Calls a procedure whose address is given in the instruction and saves their return address to the stack.

RET - Returns program execution from a procedure (subroutine) to the next instruction or main program.

IRET - Returns program execution from an interrupt service procedure (subroutine) to the main program.

- INT - Used to generate software interrupt at the desired point in a program.

INTO - Software interrupts to indicate overflow after arithmetic operation.

LOOP - Jump to defined label until CX = 0.

LOOPZ / LOOPE - Decrement CX register and jump if CX ≠ 0 and ZF = 1.

LOOPZ / LOOPNE - Decrement CX register and jump if CX ≠ 0 and ZF = 0.

Ans to the Q no - 3(b)

(b) Memory Interfacing :-

When we are executing any ~~solution~~ instruction, we need the microprocessor to access the memory for reading instruction codes and the data stored in the memory. For this both the memory and the microprocessor requires some signals to read from and write to register.

The interfacing process includes some key factors to match with the memory requirements and microprocessors signals. The interfacing circuit therefore should be designed in such a way that it matches the memory signal requirements with the signal of the microprocessor.

④ I/O Interfacing:-

There are various communication devices like the keyboard, mouse, printer, etc. So, we need to interface the keyboard, and other devices with the microprocessor by using latches and buffers. This type of interfacing is known as I/O interfacing.

The End