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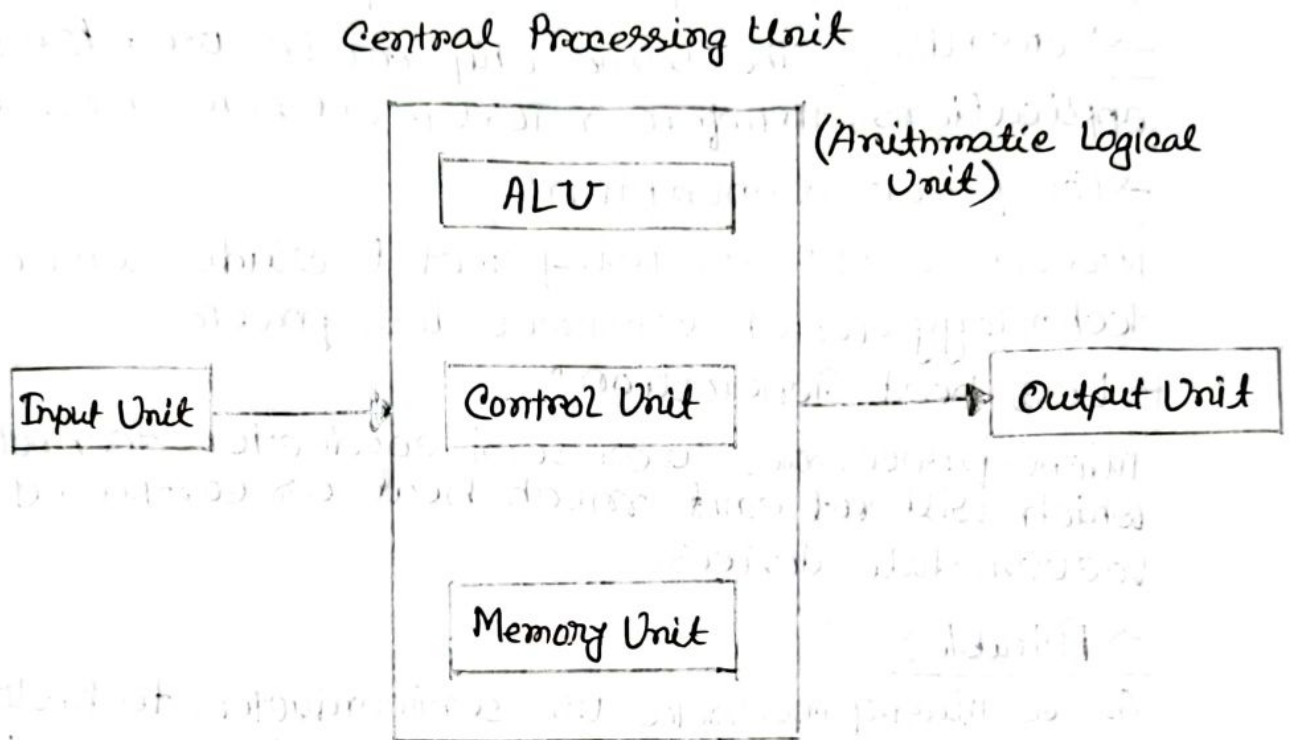
Batch : 17th

COURSE CODE : CSE 413

COURSE TITLE : Microprocessors and Interfacing

Ans to the Qus NO: 01(a)

Answer: Block Diagram of Basic Micro-computer:



Block Diagram of Computer.

Micro-processor:

Computer's central processing Unit (CPU) built on a Single Integrated Circuit (IC) is called microprocessor.

Features of Micro-processor:

- Low cost: Due to integrated circuit technology microprocessors are available at very low cost. It will reduce the cost of computer system.
- High Speed: Due to the technology involved in it the microprocessor can work at very high speed. It can execute millions of instructions per second.
- Small Size: A microprocessor is fabricated in a

Very less footprint due to very large scale and Ultra large scale integration technology. Because of this, the size of the computer size system is reduced.

→ Versatile: The same chip can be used for several applications, therefore, microprocessors are versatile.

→ Low power consumption:

Microprocessors are using metal oxide semi-conductor technology, which consumes less power.

→ Less heat generation:

Micro-processors use semi-conductor technology which will not emit much heat as compared to vacuum tube devices.

→ Reliable:

Since Microprocessors use semiconductor technology, therefore, the failure rate is very less. Hence it is very reliable.

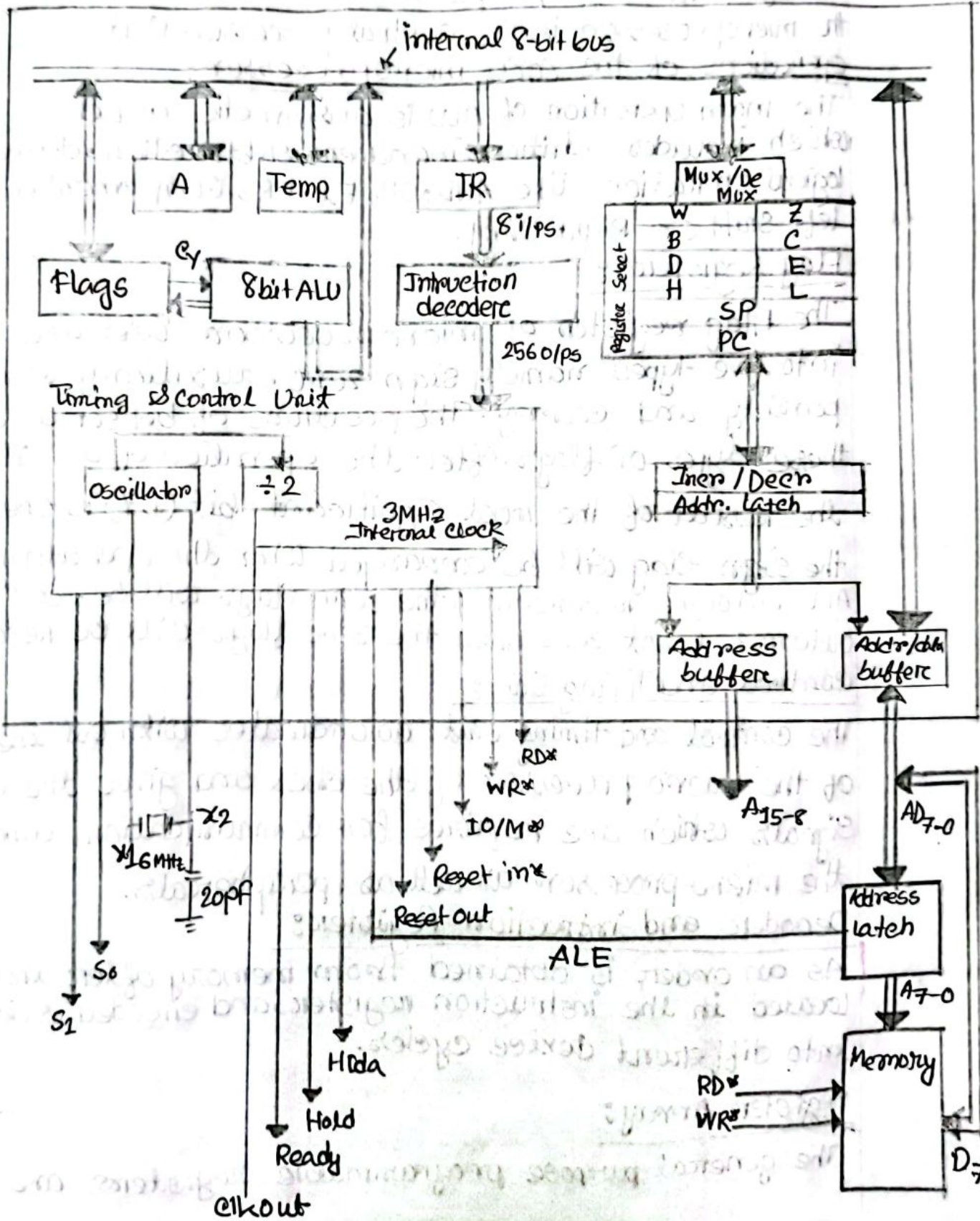
→ Portable:

Due to the small size and low power consumption Micro-processors are portable.

Ans to the Ques NO: 01 (b)

Ans:

8085 Architecture:



The architecture of the 8085 microprocessor mainly includes the timing & control unit, Arithmetic and Logic Unit, de-coder, instruction register, interrupt control, a register array, serial input/output control. The most important part of the microprocessor is the central processing unit.

operations of the 8085 microprocessor:

The main operation of ALU is arithmetic as well as logical, which includes addition, increment, subtraction, decrement, logical operations like AND, OR, Ex-OR, Complement, evaluation, left shift or Right Shift.

Flag Registers:

The Flag register of microprocessor 8085 are classified into five types namely sign, zero, auxiliary carry, parity and carry. The positions of bit set aside for these types of flags. After the operation of an ALU, when the result of the most significant bit (D7) is one, then the sign flag will be arranged. When the operation of the ALU outcome is zero then the zero flags will be set. When the outcome is not zero then the zero flags will be reset.

control and Timing Unit:

The control and timing unit co-ordinates with all the actions of the micro-processor by the clock and gives the control signals which are requires for communication among the micro-processor as well as peripherals.

Decoder and instruction Register:

As an order is obtained from memory after that it is located in the instruction register, and encoded & decoded into different device cycles.

Register Array:

The general purpose programmable registers are

classified into several types apart from the accumulator such as B, C, D, E, H & L. These are utilized as 8-bit registers otherwise coupled to stock up the 16 bit of data. W & Z are used in the processor & it cannot be utilized with the developer.

Special Purpose Registers:

These registers are classified into four types normally program counter, stack pointer, increment or decrement register, address buffer, or data buffer.

Program Counter:

This is the first type of special-purpose register and considers that the instruction is being performed by the micro-processor.
Stack Pointer in 8085:

The SP or stack pointer is a 16-bit register and functions similar to a stack, which is constantly increased or decreased with two throughout the push and pop process.

Increment or Decrement Register:

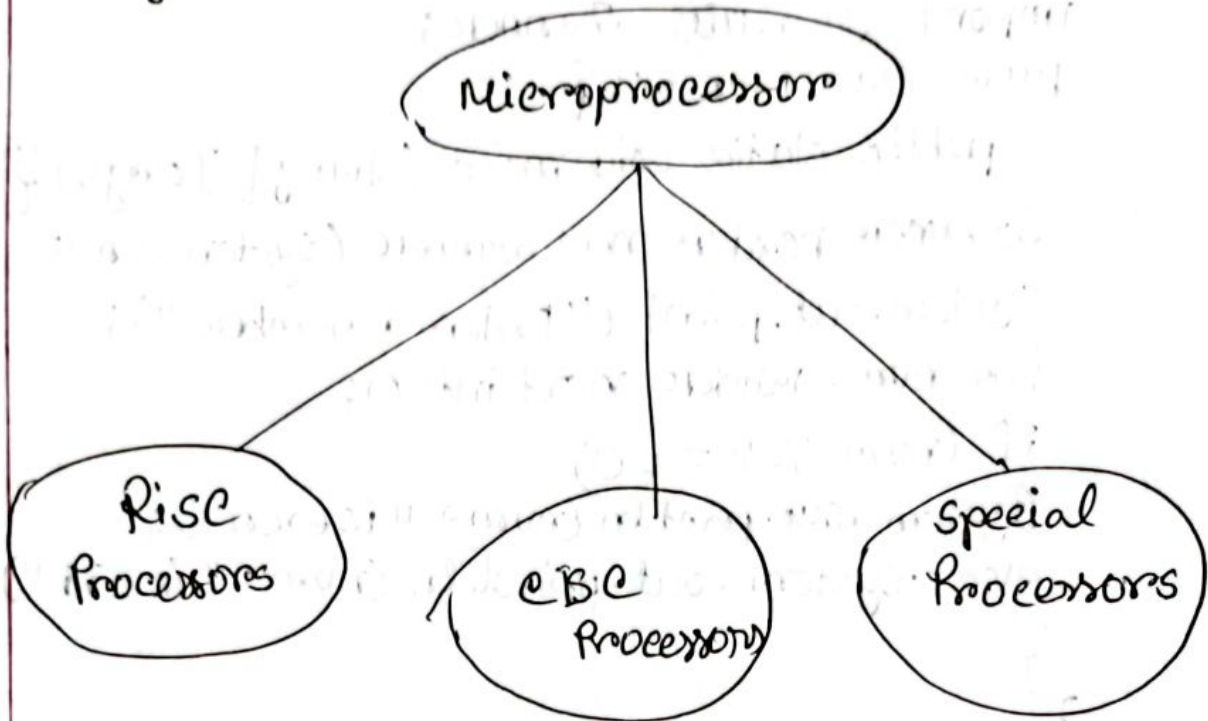
8-bit register contents can be increased or decreased
16 bit register useful for incrementing or decrementing
program counters as well as stack pointer register

Address buffer & Address data buffers:

It stores the copied information from the memory for the execution. The memory & I/O chips are associated with these buses, then the CPU can replace the preferred data by I/O chips and the memory.

Ans to the Qus No: 01 (c)

Ans: A microprocessor can be classified into three categories-



RISC Processors:

RISC stands for Reduced Instruction Set Computer. It is designed to reduce the execution time by simplifying the the instruction set of the computer.

Using RISC processors, each instruction requires only one clock cycle to execute results in uniform execution time. This reduces the efficiency as there are more lines of code, hence more RAM is needed to store the instructions. The compiler also has to work more to convert high-level language instructions into machine code. Some of the RISC Processors are:

- Power PC: 601, 604, 615, 620
- PA-RISC: HP 7100LC.

CISC Processor:

CISC stands for Complex Instruction Set Computer. It is designed to minimize the number of instructions per program, ignoring the number of cycles per instruction. The emphasis is on building complex instructions directly into the hardware.

The compiler has to do very little work to translate a high-level language into assembly level language machine code because the length of the code is relatively short, so very little RAM is required to store the instructions.

Some of the CISC processors are -

- IBM 370/168
- VAX 11/780.

Special processor:

These are the processors which are designed for some special purposes. Few of the special processors are briefly discussed -

Co-processor:

A co-processor is a specially designed microprocessor, which can handle its particular function many times faster than the ordinary micro-processor.

For example - Math co-processor.

Some Intel Math-coprocessors are -

☐ 8087 - used with 8086

☐ 80287 used with 80286

Input/output processor:

It is a specially designed microprocessor having a local memory of its own, which is used to control I/O device with minimum CPU involvement.

Ans to the Qus NO: 02 (a)

Ans: Initially when any device has to send data between the device and the memory, the device has to send DMA Request (DRQ) to DMA controller.

→ DMA controller sends hold request (HOLD) to the CPU and waits for the CPU to assert the HLDA.

→ Then the microprocessor tri-states all the data bus, address bus and control bus. The CPU leaves the control over bus and acknowledges the HOLD request through HIDA signal.

→ Now the CPU is in HOLD state and the DMA controller has to manage the operations over buses between the CPU, Memory and I/O devices.

Ans to the Qus NO: 02 (b)

Ans: Features of 8257:

→ It has four channels which can be used over four I/O devices.

→ Each channel has 16 bit address and 14-bit counter.

→ Each channel can transfer data upto 64Kb.

→ Each channel can be programmed independently.

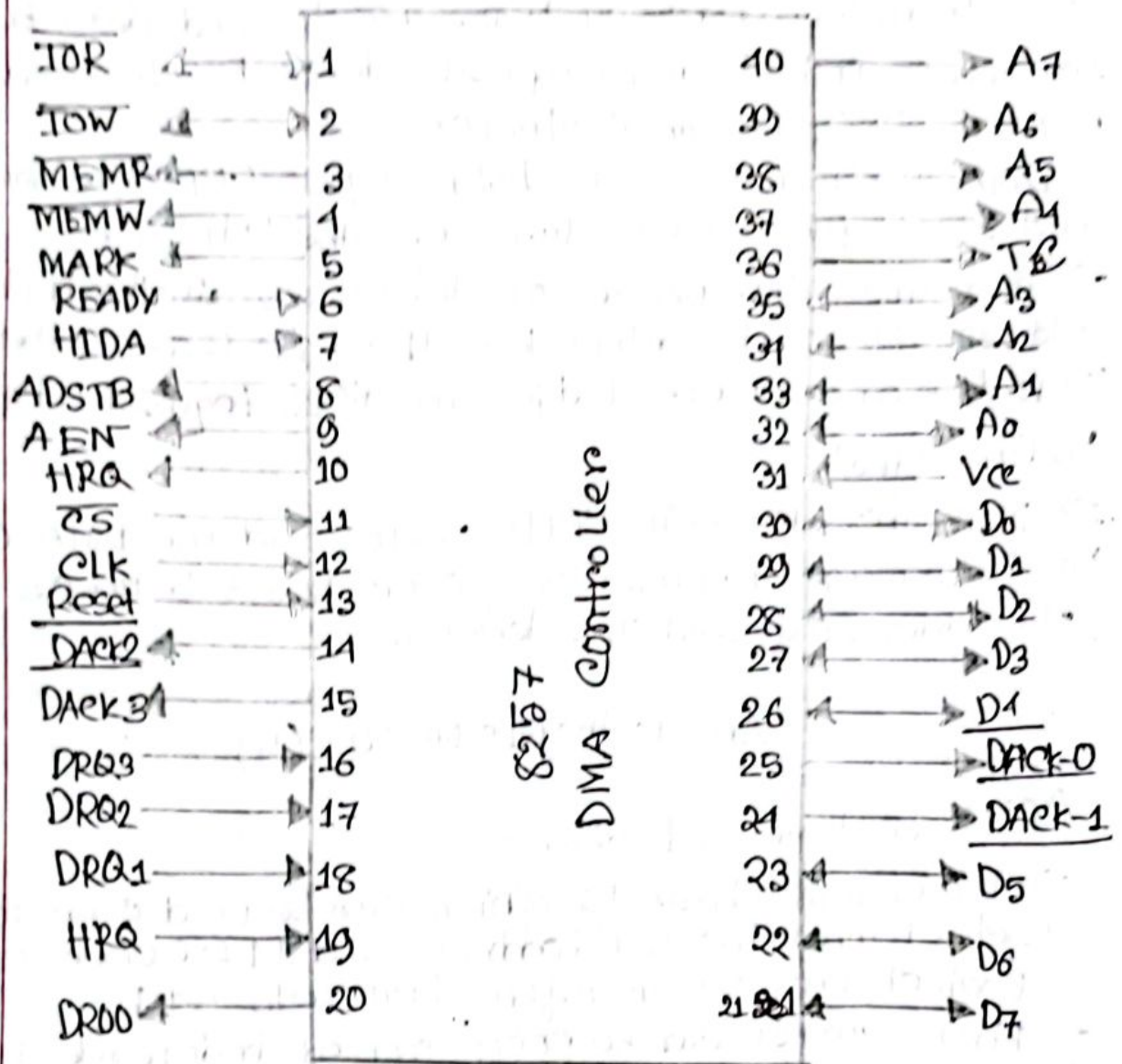
→ Each channel can perform read-transfer, write transfer and verify-transfer operations.

→ It generates MARK signal to the peripheral device that 128 bytes have been transferred.

→ It requires a signal phase clock.

→ Its frequency ranges from 250KHz to 3MHz.

→ It operates in 2 modes, Master mode & slave Mode.



Pin Diagram of 8257

DRQ0 - DRQ3 :

These are the four individual channel DMA request inputs, which are used by the peripheral devices for using DMA services. When the fixed priority

mode is selected, then DRQ₀ has the highest priority and DRQ₃ has the lowest priority among them.

DAK₀ - DAK₃ :

These are the active low DMA acknowledge lines, which updates the requesting peripheral about the status of their request by the CPU. These lines can also act as strobe lines for the requesting devices.

D₀ - D₇ :

These are bidirectional, data lines which are used to interface the system bus with the internal data bus of DMA controller. In the slave mode, it carries command words to 8257 and status word from 8257. In the master mode, these lines are used to send higher byte of the generated address to the latch. This address is further latched using ADSTB signal.

IOR :

It is an active-low bidirectional tri-state input line, which is used by the CPU to read internal registers of 8257 in the slave mode. In the Master mode, it is used to read data from the peripheral devices during a memory write cycle.

IOW :

It is an active low bi-direction tri-state line, which is used to lead the contents of the data bus to the 8-bit mode register or upper/lower byte of a 16-bit DMA address register or terminal count registers.

CLK: It is a clock frequency signal which is required for the internal operation of 8257.

RESET:

This signal is used to RESET the DMA controller by disabling all the DMA channels.

A₀-A₃ :

These are the four least significant address lines. In the slave mode, they act as an input which selects one of the registers to be read or written. In the master mode, they are the four least significant memory address output lines generated by 8257.

CS :

It is an active-low chip select line. In the slave mode, it enables the read/write operations to/from 8257.

In the master mode, it disables the read/write operations to/from 8257.

A₄-A₇ :

These are the higher nibble of the lower byte address generated by DMA in the master mode.

READY :

It is an active-high asynchronous input signal, which makes DMA ready by inserting wait states.

HRQ :

This signal is used to receive the hold request signal from the output device. In the slave mode, it is connected with a DRQ input line 8257. In Master mode, it is connected with HOLD input of the CPU.

HLDA:

It is the hold acknowledgement signal which indicates the DMA Controller that the bus has been granted to the requesting peripheral by the CPU when it is set to 1.

MEMR:

It is the low memory read signal, which is used to read the data from the addressed memory locations during DMA read cycles.

MEMW:

It is the active-low three state signal which is used to write the data to the addressed memory location during DMA write operation.

ADST:

This signal is used to convert the higher byte of the memory address generated by the DMA Controller into the latches.

AEN:

This signal is used to disable the address bus/data bus.

TC:

It stands for "Terminal Count" which indicates the present DMA cycle to the present peripheral devices.

MARK:

The mark will be activated after each 128 cycles or integral multiples of it from the beginning. It indicates the current DMA cycle is the 128th cycle since the previous MARK output to the selected peripheral device.

Vcc:

It is the power signal which is required for the operation of the circuit.

Ans to the Qus NO: 03 (a)

Ans: Rotate Instructions:

The following instructions come under this category :

Instruction	Description
RCL	Rotate all bits of the operand left by specified number of bits through carry flag.
RCR	Rotate all bits of the operand right by specified number of bits through carry flag.
ROL	Rotate all bits of the operand left by specified number of bits.
ROR	Rotate all bits of the operand right by specified number of bits.

Shift Instructions:

The following instructions come under this category:

Instructions	Descriptions:
SAL or SHL	Shifts each bit of operand left by specified number of bits and put zero in LSB position.
1 SAR	Shifts each bit of any operand right by specified number of bits. Copy old MSB into new MSB.

Branch Instructions:

The following instructions come under this category:

Instructions	Description
JA or JNBE	Jump if above, not below, or equal i.e. when CF and $ZF=0$
JAE/JNB/JNC	Jump if above, not below, equal or no carry i.e. when $CF=0$
JB/JNBE/JC	Jump if below, not above, equal or carry, i.e. when $CF=0$
JBE/JNA	Jump if below, not above, or equal i.e. when $CF=ZF=1$
JEXZ	Jump if ex register = 0
JE/JZ	Jump if zero or equal i.e. when $ZF=1$
JG/JNLE	Jump if greater, not less or equal i.e. when $ZF=0$ and $CF=0F$
JGE/JNL	Jump if greater, not less or equal i.e. when $SF=0F$
JL/JNBE	Jump if less, not greater than, or equal i.e. when SF $SF \neq 0F$
JLE/JNG	Jump if less, equal or not greater i.e. when $ZF=1$ and $SF \neq 0F$
JMP	Causes the program execution to jump unconditionally to the memory address or label given in the instructions.

Ans to the Qus NO: 03 (b)

Ans: Memory interfacing: When we are executing any instruction, the address of memory location or an I/O device is selected by the microprocessor. The corresponding memory chip or I/O device is selected by a decoding circuit. Memory requires some signals to read from and write to registers and microprocessor transmits some signals for reading or writing data. The interfacing process includes matching the memory requirements with the microprocessor signals.

I/O Interfacing:

As we know, keyboard and displays are used as communication channels with outside world. Therefore, it is necessary that we interface keyboard and displays with the microprocessor.

This is called I/O interfacing for this type of interfacing. We use latches and buffers for interfacing the keyboards and displays with the microprocessor.