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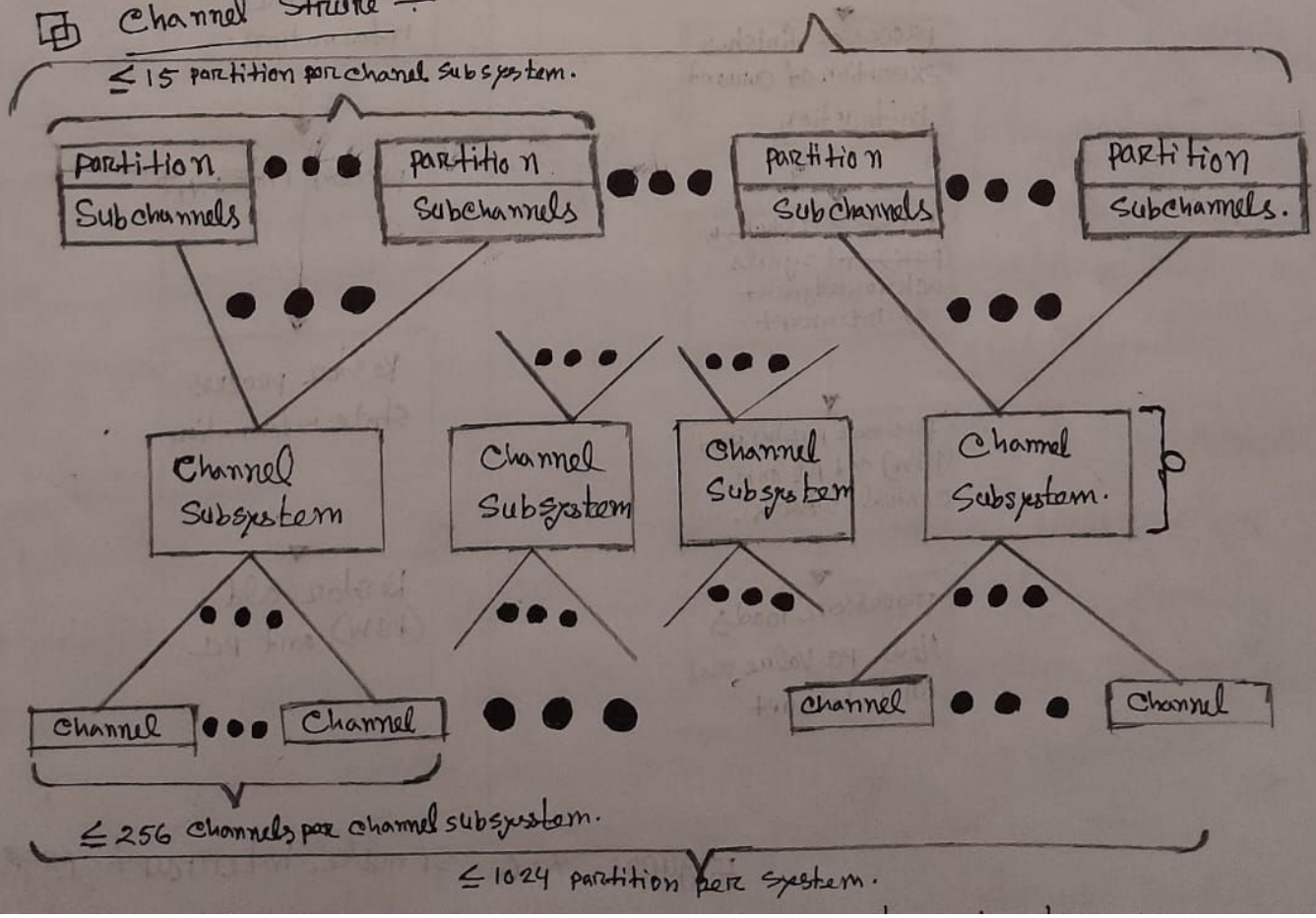
Subject: Computer Architecture.

Code – CSE 313.

Answer to the Question No – 01 (a)

Answer: **IBM z EC12 I/O channel subsystem:** The z enterprise EC12 is IBM's latest Mainframe Computer Offering (At the time of this writing). This system is based on the use of the z EC12 prossesor chip, which is a 5.5- GHz Multicore chip with six Cores. The z EC12 architecture can have maximum of 101 prossesor chip with 6 cores.

Channel Struure :-



① ⓑ Answer: I/O Divice Completes an I/O oparonts sequence of Hardware:

The Occurence of an interrupt triggers a number of events, Both in the proces Hardware And in Software. Figure 7.6 shows a typicale sequeneal. When an I/o device Completes an I/O Operation. the following Squence of Hardware events occurs.

- The Divice issues an interrupt signal to the prosseson.
- The prosseson finiskes execution of the Current Instruction befor responding to the interrupt, as indicated in fi.
- (Software)

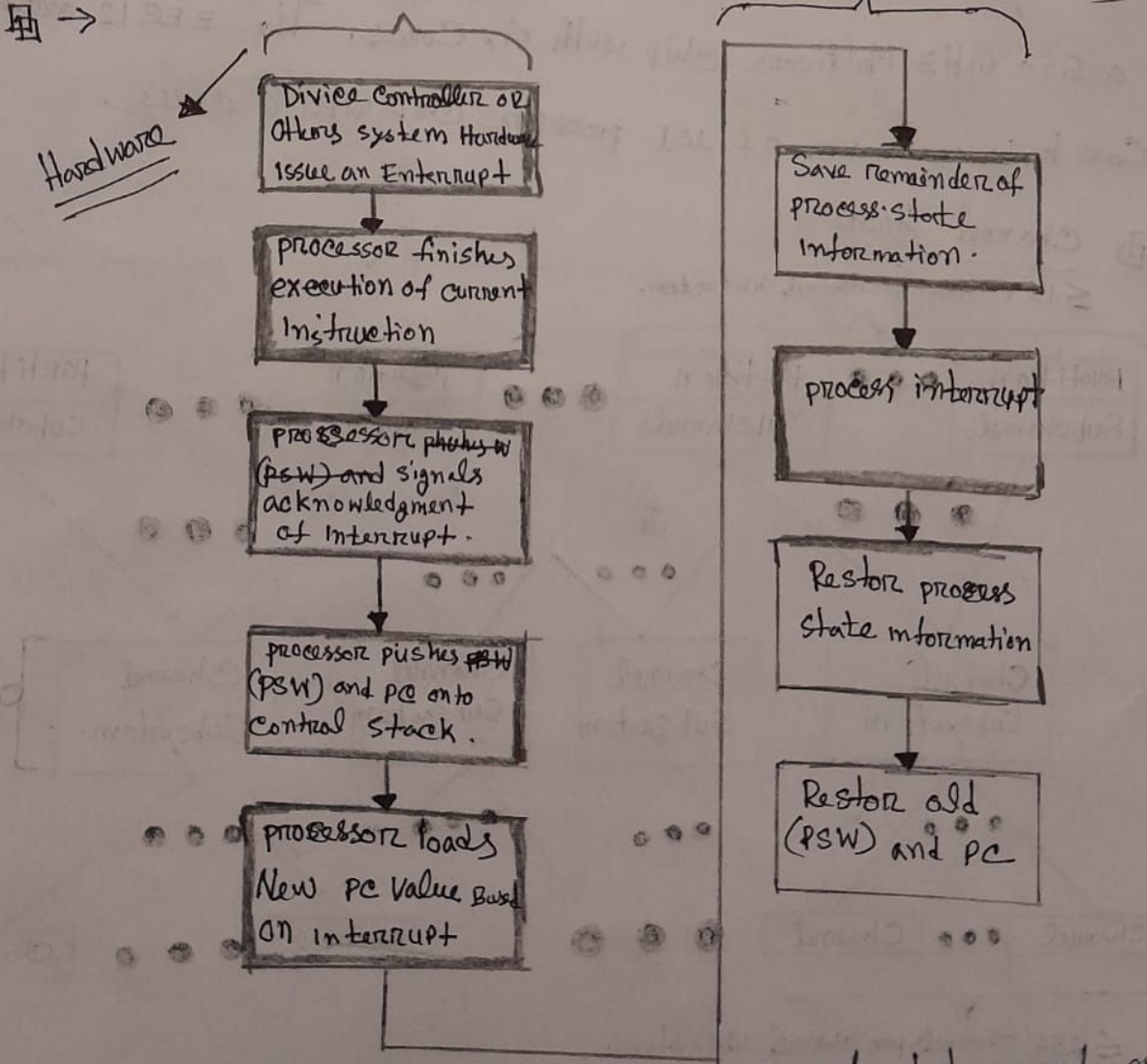


Figure: 7.6 Simple Interrupt processing.

⊞→ The processor now Needs to prepare to transfer to transfer Control to the interrupt routine. To Begin. it Needs to save Information Needed to Resum the Current program at the point of Interrupt. The minimum information required is (a) the status Of the processor which Contained in a register called the program status word (PWS) and (b) the location of the ~~nes~~ Next Instruction to be Executed wich is Contained in the pogram. Counter. Thes can be pushed on to the sqystem Control stack.

⊞→ The processor Now loads the program Counter with the entry location of the Interrupt-handling program that will respond to this interrupt. Depending, On the Computer Architecture and Operating System design. there may be a Single program On program for each type of interrupt; or on one program for each devicee and each type of interrupt. If there is more then on Interrupt handdleaning routin. the processor must ~~det~~ determind which one to invoke. The information may have been include in the original Interrupt signal. or the processor may have to issue a request to the Dirice that issued the interrupt to get a response that Contains the needed information.

⊞→ At this point, the program Counter And (PSW) relating to the interrupted program have been saved On the System Stack. However, there is other information that is Considered part of the "state" of the Executing program. In particular, the Contents of the processor registers Need. as to be saved, because thes registers may be used by interrupt handle. So all of thes values ~~plus~~ plus Any Other stat Information, need to be saved. Typically, the interrupt handler

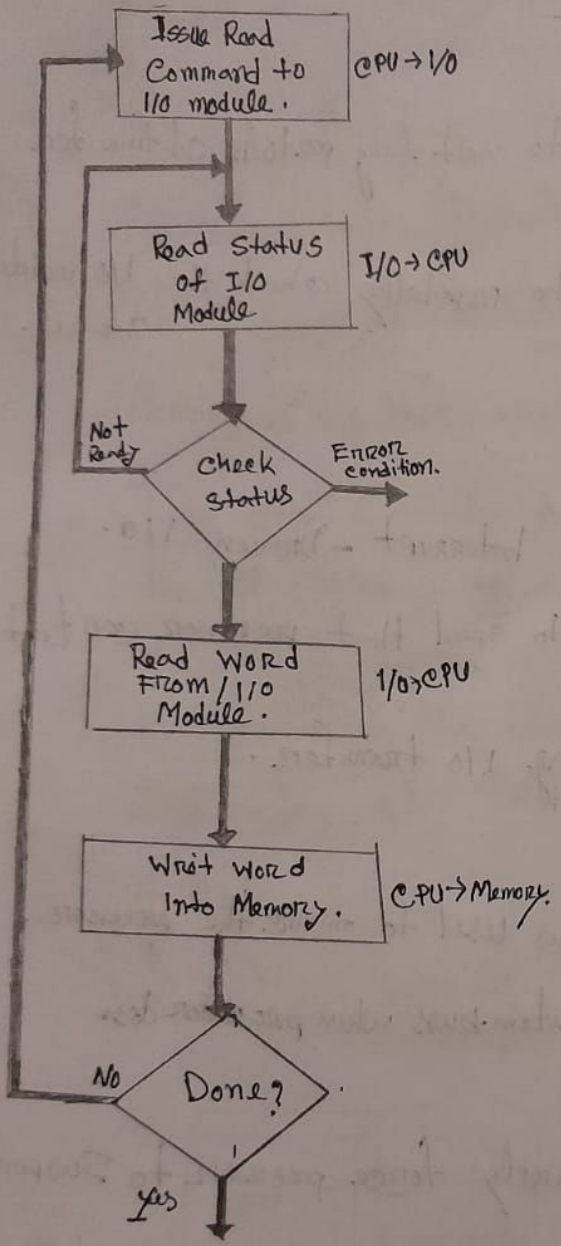
⊞→ The Interrupt handler next processes the Interrupt. This includes an Examination Of Status information relating to the I/O Operation or Other event that caused an Interrupt. It may Also involve Sending Additional Commands or Acknowledgment to the I/O Device.

⊞→ When Interrupt processing in Completed the save register values are Retrieved from the Stack And Restor to the Registor.

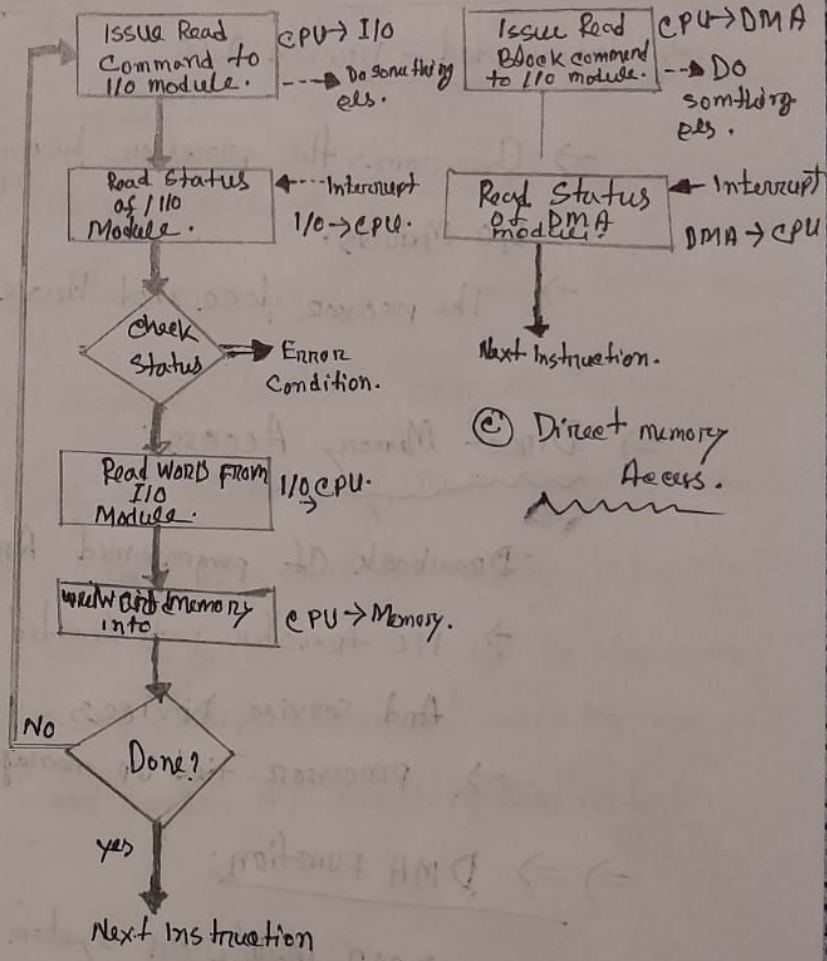
⊞→ The final Act is to restor the (PSW) And program Counter value from the Stack. As Result, the next instruction to be Executed will be from the previously interrupted program.

Note that it is important to save all the state information About the Interrupted program for letter resumption. This is because the Interrupt is not a routin called from the program. Rather the Interrupt can occur At any ⊞ time and therefor At any point in program. the Execution of a user program. Its occurrence is unpredictable Indeed, as we will see in the next chapter the two programs may not Have Anythings in Common And may belong to two different User.

© Ans: Three Techniques for input Of Block Diagram Describe:



(a) programI/o.



(b) Interrup-Driven I/O.

(c) Direct memory Access.

⇒⇒ Three Techniques for input of Block Data.

I/O-Instruction: processor views I/O operation in a similar manner as Memory operations. Each Device is given a unique identifier or Address. processor issue Commands Containting Device Address - I/O module must Cheak Address line to See if the Command is for itself.

⇒ I/O mapping:
- → Memory - mapped I/O
- → Isolated I/O.

⇒ Interrupted - Driven I/O

→ Overcomes the processor having to wait long periods of time for I/O Modules.

→ The processor dose not Have to repetadly check the I/O module status.

⇒ Direct Memory Access.

Drawback of programmed And Interrupt - Driven I/O.

→ I/O transfer rate limited to speed that processor can test And service Devices.

→ Processor tied up managing I/O transfer.

⇒ ⇒ DMA Function:

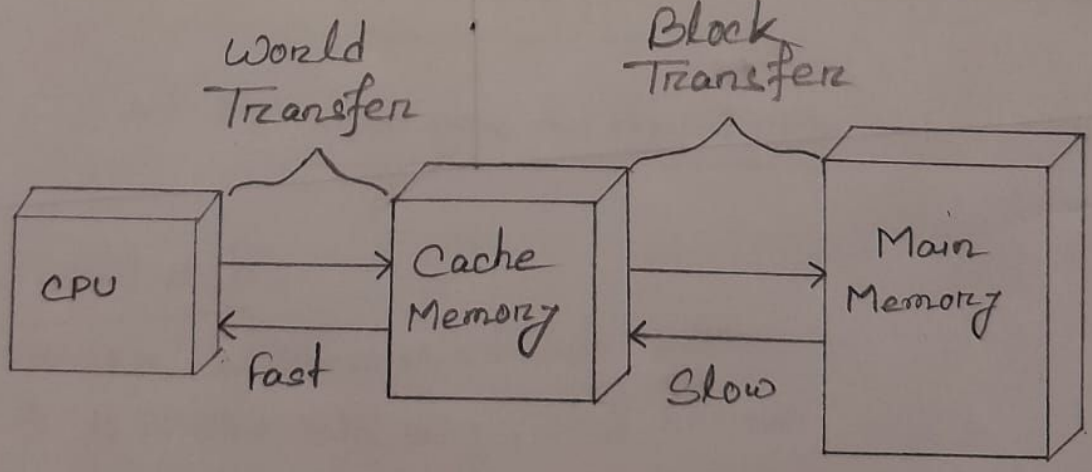
→ DMA Module on system bus used to mimic the processor.

→ DMA Module Only used System-buss when processor dose Does not need. It.

→ DMA Module may temporarily force processor to Suspend Operation - cycle stealing.

Answer to the Question No-2

2/ ⓐ Answer: Cache Memory/main memory Cache Memory is Designed to combine. the Memory Access time of Expensive, high-speed Memory Combined with the large Memory Size of less Expensive, lower-speed Memory. The Concept is illustrated. There is a relatively large & slow main Memory together with a smaller, faster cash Memory. The cash Contains a Copy of portions of main memory. When the processor attempts to read a word of memory check is Made to Determine if the word is in the cash. If so the word is delivered to the processor. If not a Block of main Memory, Consisting of Some fixed Number of word, is Read into the cash



The cache is much faster and more Expensive the main memory. However, both of these Computer Memories are Directly accessible by the processor.

⇒ ⇐ Basic of Comparison:

purpose	Cache memory	Main Memory.
purpose	it is used to store frequently used Data.	it holds the Data that is Curently being processed.
Access	Comparatively faster than memory.	It is also the faster Accessing memory.
Cost	More Expensive then main Memory.	Expensive Memory.
Size	Comparatively smaller then Main Memory.	Large then Cach memory.
Type	L1, L2, L3	SRAM And DRAM

② ⓑ Answer Logical And physical caches Describe!

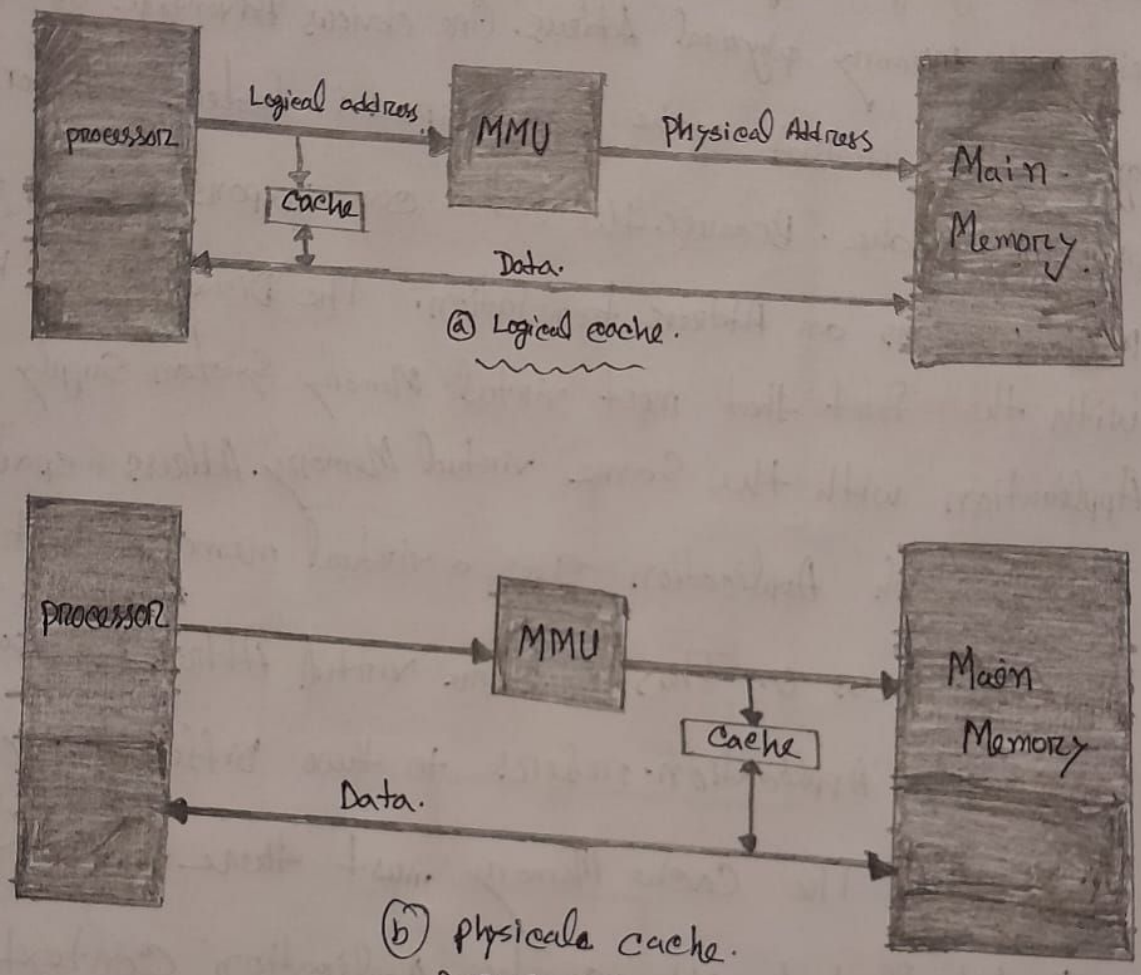


Fig: Logical cache And physical cache.

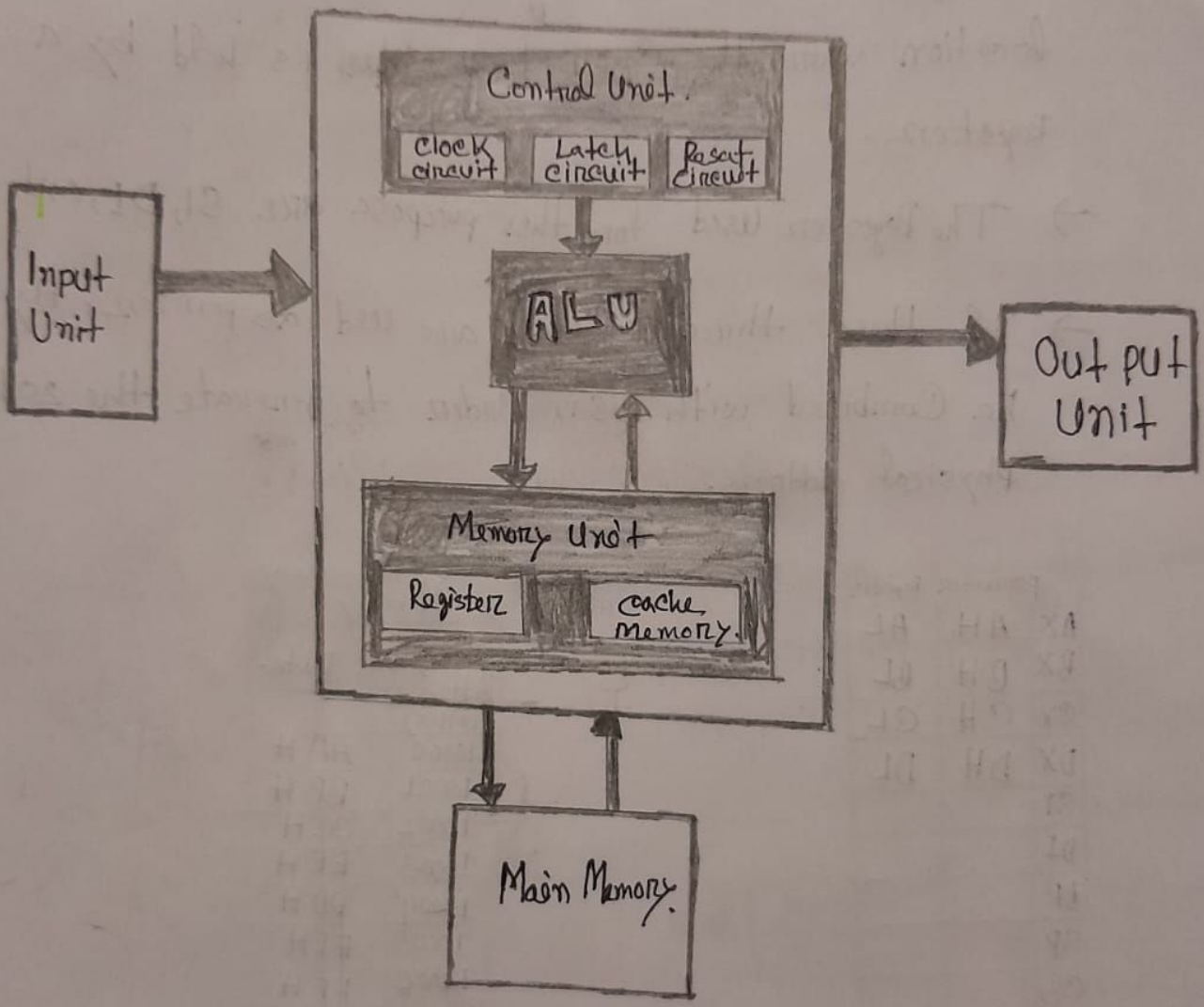
⇒⇒ Logical cache:

→ It is also known as a virtula cache.
→ It is stor Data using virtual Addresses.
⇒ The processor Access cache Directly without going through MMU.
→ Advantage: It is faster then physical cache, Because the cache can respond befor the MMU performs An Address translation.

⇒ physical caches: The processor Access the cache directly without going through the MMU. A physical caches stores Data using main Memory physical Address. One obvious Advantage of the logical cache it that cache Access spead is faster then for a physical cache. Because the cache can Respons before the MMU performs an Address translation. The Disadvantage his to do with the fact that most virtual Memory System supply each Application with the same virtual Memory. Address space. That is each Application sees a virtual memory that start At Address 0. Thus the same virtual Address in two Different Application refers to two different physicle Address. The Cache Memory must there for be Completly ~~flushed~~ flushed with cache Application Context.

Answer to the Question NO - 3 (a)

(3) (a) Ans: Central processing unit (CPU)



⇒⇒ Central processing main unit :

- → Control unit
  - clock circuit.
  - Latch "
  - Resat "
- → Arithmatic & Logical unit (ALU)
- → Memory unit
  - Register
  - cache memory.

3 (b) Ans:

x86 Addressing Mode Indirect:

→ In register indirect Addressing Mode, the Address of the Memory location where the Operand resides is held by a Register.

→ The Register used for this purpose are SI, DI, and BX.

→ If these three register are used as pointer, they must be Combined with DS in Order to generate the 20 bit physical Address.

Processor Register		
AX	AH	AL
BX	BH	BL
CX	CH	CL
DX	DH	DL
SI		
DI		
BP		
SP		
CS		
DS		
SS		
ES		

Memory	
Memory Address (in Hex)	Data
10000	AA H
10001	BB H
10002	CC H
10003	EE H
10004	DD H
10005	EE H
10006	FF H
10007	11 H
10008	22 H
10009	33 H
1000A	44 H