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Microprocessor CSE-413

Final Assessment

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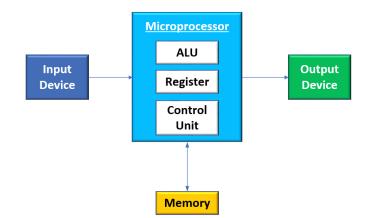
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Answer to the Question No- 1 (a)



Block Diagram of a basic Microcomputer:

Block diagram of Micro Computer shows here. Microcomputer was once a frequent word for personal computers, specifically for a class of compact digital computers using a single integrated semiconductor chip as the CPU.

Features of Microprocessor: Microprocessor is used in a variety of applications due to their unique features such as size, weight, cost, high computing power, and low power consumption, etc., Microprocessor fitted systems are used.

- to monitor and control operations of Industrial devices by measuring key parameters like temperature, pressure, speed.
- in instruments to raise an alert or warning on extreme conditions.
- to automate office work/business processes and improve white collar productivity.
- in simplifying publishing activity.
- to speed up the information exchange through Telephone and Satellite network.
- in rolling out innovations in entertainment, games and Photography.
- to make everybody and everything stay connected with each other.

Answer to the Question No- 1 (b)

Intel 8085 is fabricated as a 40-pin DIP IC. DIP stands for 'dual inline package'. It means the package will have pins on only two sides, 20 on each side in this case.

Intel manufactures 8085 in several versions, like 8085A, 8085AH, 8085AH-2, and 8085AH-1. The 8085A is fabricated using NMOS technology. It is a variant of MOS (metal oxide semiconductor) technology. It uses n channel silicon-gate process. The AH series are more expensive processors, which use high-density MOS (HMOS) for fabrication. They typically consume 20% less power compared to the A series.

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X1	\rightarrow	1		40	← Vcc
X2	\rightarrow	2		39	← Hold
Reset out	4	3		38	→ HLDA
SOD	4	4		37	→ Clk out
SID	\rightarrow	5		36	← Reset in
Trap	\rightarrow \rightarrow	6		35	← Ready
RST 7.5	\rightarrow	7		34	→ I0/M*
RST 6.5	\rightarrow	8		33	→ SI
RST 5.5	\rightarrow	9		32	→ RD*
INTR	\rightarrow	10	8085	31	→ WR*
INTA*	4	11		30	→ ALE
ADO	\leftrightarrow	12		29	\rightarrow so
AD1	\leftrightarrow	13		28	→ A15
AD2	\leftrightarrow	14		27	\rightarrow A14
AD3	\leftrightarrow	15		26	→ A13
AD4	\leftrightarrow	16		25	→ A12
AD5	\leftrightarrow	17		24	→ A11
AD6	\leftrightarrow	18		23	→ A10
AD7	\leftrightarrow	19		22	→ A9
Vss	\rightarrow	20		21	→ A8
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Pin diagram of 8085

Answer to the Question No- 1 (c)

Microprocessors can classify based on their application & architecture of microprocessors. Based on the application of the processors, they are classified as-

- General Purpose Processors
- ➢ Microcontrollers
- Special Purpose Processors

Based on the architecture of the processor, they are classified as-

- RISC (Reduced Instruction Set Computer)
- CISC (Complex Instruction Set Microprocessors)

General Purpose Processor

- The use of general-purpose processors by the programmer for any application is used in general computer system integration.
- Common microprocessors such as Intel 8085 to Intel Pentium processors are an example of general-purpose processors.

Microcontroller

- The microcontrollers are the microprocessor designed especially for control applications.
- Microcontrollers contain memory units and I/O ports inside a chip in addition to the CPU part.
- Some of the machines using microcontrollers are microwave ovens, washing machines, computer printers, fax machines, etc.

Special Purpose Processor

- Special-purpose processors are designed specifically to handle special functions required for an application.
- Digital signal processors are examples of special-purpose processors and these have special instructions to handle signal processing.
- The application-specific integrated circuits chips are also examples of this category of microprocessors.

RISC (Reduced Instruction Set Computer)

- RISC stands for Reduced instruction set computer. RISC chips evolved around mid -1980 as a reaction to CISC chips.
- It is designed to reduce the execution time by simplifying the instruction set of the computer.
- Using RISC processors, each instruction requires only one clock cycle to execute results in uniform execution time.
- This reduces the efficiency as there are more lines of code, hence more RAM is needed to store the instructions.
- The compiler also has to work more to convert high-level language instructions into machine code.
- Because of the Simpler and faster instructions, RISC chips have more simple instructions due to this require fewer transistors, which makes them easier to design and cheaper to produce.

CISC (Complex Instruction Set Microprocessors)

- CISC stands for Complex Instruction Set Computer.
- It is designed to minimize the number of instructions per program, ignoring the number of cycles per instruction.
- The more focus is on building complex instructions directly into the hardware.
- The compiler has to do very little work to translate a high-level language into assemblylevel language/machine code because the length of the code is relatively short, so very little RAM is required to store the instructions
- most PC use CPU based on architecture. For instance, intel and AMD CPU are based on CISC architectures.

Answer to the Question No- 2 (a)

DMA stands for Direct Memory Access. It is designed by Intel to transfer data at the fastest rate. It allows the device to transfer the data directly to/from memory without any interference of the CPU.

Using a DMA controller, the device requests the CPU to hold its data, address and control bus, so the device is free to transfer data directly to/from the memory. The DMA data transfer is initiated only after receiving HLDA signal from the CPU.

Following is the sequence of operations performed by a DMA-

- Initially, when any device has to send data between the device and the memory, the device has to send DMA request (DRQ) to DMA controller.
- The DMA controller sends Hold request (HRQ) to the CPU and waits for the CPU to assert the HLDA.
- Then the microprocessor tri-states all the data bus, address bus, and control bus. The CPU leaves the control over bus and acknowledges the HOLD request thro ugh HLDA signal.
- Now the CPU is in HOLD state and the DMA controller has to manage the operations over buses between the CPU, memory, and I/O devices.

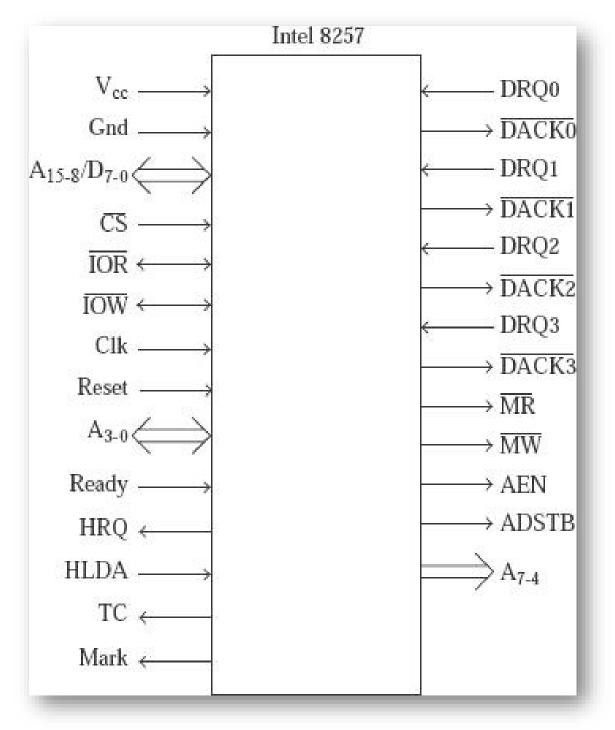
Answer to the Question No- 2 (b)

The 8257 pins are described is given below-

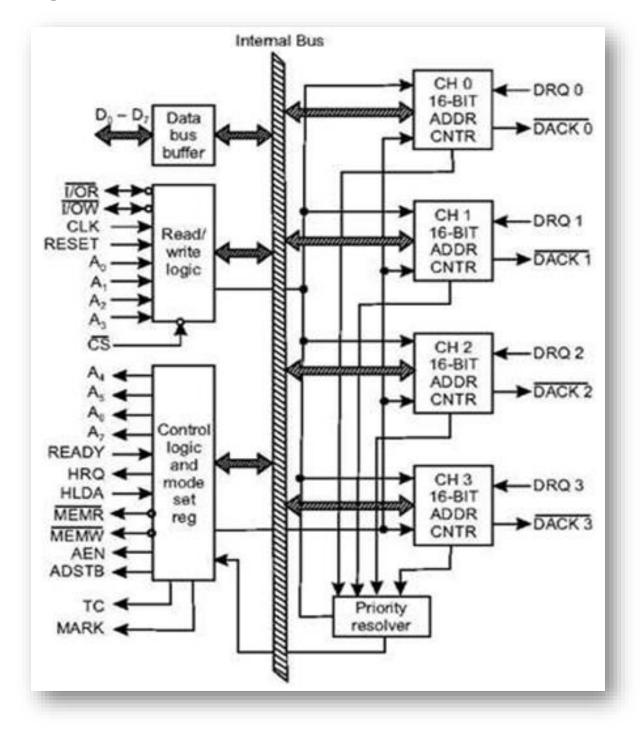
Physical pin diagram of Intel 8257:

	Intel 8257	40-pin DIP
$\overline{IOR} \longleftrightarrow 1$	40	$\rightarrow A_7$
$\overline{IOW} \longleftrightarrow 2$	39	$\rightarrow A_6$
$\overline{MR} \leftarrow 3$	38	$\rightarrow A_5$
$\overline{\text{MW}} \leftarrow 4$	37	$\longrightarrow A_4$
Mark ← 5	36	\rightarrow TC
Ready \longrightarrow 6	35	$\leftrightarrow A_3$
$HLDA \longrightarrow 7$	34	$\leftrightarrow A_2$
$ADSTB \leftarrow 8$	33	$\leftrightarrow A_1$
$AEN \leftarrow 9$	32	$\leftrightarrow A_0$
$HRQ \leftarrow 10$	31	$\leftarrow V_{cc}$
$\overline{CS} \longrightarrow 11$	30	$\leftrightarrow D_0/A_8$
$Clk \longrightarrow 12$	29	$\leftrightarrow D_1/A_9$
Reset \longrightarrow 13	28	$\leftrightarrow D_2/A_{10}$
$DACK2 \leftarrow 14$	27	$\leftrightarrow D_3/A_{11}$
$\overline{\text{DACK3}} \leftarrow 15$	26	$\leftrightarrow D_4/A_{12}$
$DRQ3 \longrightarrow 16$	25	$\rightarrow \overline{\text{DACK0}}$
$DRQ2 \longrightarrow 17$	24	\rightarrow DACK1
$DRQ1 \longrightarrow 18$	23	$\leftrightarrow D_5/A_{13}$
$DRQ0 \rightarrow 19$	22	$\leftrightarrow D_6/A_{14}$
$Gnd \longrightarrow 20$	21	$\leftrightarrow D_7/A_{15}$
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Functional pin diagram of Intel 8257:



8257 pin Architecture:



Answer to the Question No- 3 (a)

As we know that any machine (system) works on machine language, which consists of binary numbers. In the 8086 microprocessors, we have 16-bit registers to handle our data.

Rotate Instructions

Instruction	Description			
RCL	Rotate all bits of the operand left by specified number of bits through carry flag.			
RCR	Rotate all bits of the operand right by specified number of bits through carry flag.			
ROL	Rotate all bits of the operand left by specified number of bits.			
ROR	Rotate all bits of the operand right by specified number of bits.			

The following instructions come under this category:

Shift Instructions

The following instructions come under this category:

Instruction	Description
SAL or SHL	Shifts each bit of operand left by specified number of bits and put zero in LSB position.
SAR	Shift each bit of any operand right by specified number of bits. Copy old MSB into new MSB.
SHR	Shift each bit of operand right by specified number of bits and put zero in MSB position.

Branch Instructions

It is also called program execution transfer instruction. Instructions of this group transfer program execution from the normal sequence of instructions to the specified destination or target. The following instructions come under this category:

Instruction	Description	
JA or JNBE	Jump if above, not below, or equal i.e. when CF and $ZF = 0$	
JAE/JNB/JNC	Jump if above, not below, equal or no carry i.e. when $CF = 0$	
JB/JNAE/JC	Jump if below, not above, equal or carry i.e. when $CF = 0$	
JBE/JNA	Jump if below, not above, or equal i.e. when CF and $ZF = 1$	
JCXZ	Jump if CX register = 0	
JE/JZ	Jump if zero or equal i.e. when $ZF = 1$	
JG/JNLE	Jump if greater, not less or equal i.e. when $ZF = 0$ and $CF = OF$	
JGE/JNL	Jump if greater, not less or equal i.e. when SF = OF	
JL/JNGE	Jump if less, not greater than or equal i.e. when $SF \neq OF$	
JLE/JNG	Jump if less, equal or not greater i.e. when $ZF = 1$ and $SF \neq OF$	
JMP	Causes the program execution to jump unconditionally to the memory address or label given in the instruction.	
CALL	Calls a procedure whose address is given in the instruction and saves their return address to the stack.	
RET	Returns program execution from a procedure (subroutine) to the next instruction or main program.	
IRET	Returns program execution from an interrupt service procedure (subroutine) to the main program.	
INT	Used to generate software interrupt at the desired point in a program.	
ΙΝΤΟ	Software interrupts to indicate overflow after arithmetic operation.	
LOOP	Jump to defined label until $CX = 0$.	
LOOPZ/LOOPE	Decrement CX register and jump if $CX \neq 0$ and $ZF = 1$.	
LOOPNZ/LOOPNE	Decrement CX register and jump if $CX \neq 0$ and $ZF = 0$.	

Here, CF = Carry Flag

- ZF = Zero Flag
- OF = Overflow Flag
- SF = Sign Flag
- CX = Register

Answer to the Question No- 3 (b)

Memory refers to the storage units where data and instructions are temporarily stored for processing by the microprocessor. There are two main types of memory in microprocessors:

- 1. Random Access Memory (RAM): RAM is volatile memory that can be read from and written to by the microprocessor. It is used for temporary storage of data and instructions, and the contents of RAM are lost when the power is turned off.
- 2. Read-Only Memory (ROM): ROM is non-volatile memory that can only be read by the microprocessor. It is used to store permanent data and instructions, such as the program that starts up when the computer is turned on.

There are various types of RAM and ROM, including Dynamic RAM (DRAM), Static RAM (SRAM), Programmable ROM (PROM), and Erasable Programmable ROM (EPROM). Each type of memory has different characteristics, such as cost, speed, and capacity, which make them suitable for different applications.

I/O (**Input/Output**) **interfacing** refers to the communication between the microprocessor and the external devices such as keyboards, displays, storage devices, etc. The microprocessor communicates with these devices by sending and receiving data and control signals through an I/O interface.

There are two main methods of I/O interfacing:

Memory-Mapped I/O: In this method, I/O devices are assigned memory addresses, just like memory. The microprocessor reads and writes data to these memory addresses, which are then passed on to the corresponding I/O device. This method is simple and efficient, but it uses valuable memory space.

Port-Mapped I/O: In this method, I/O devices are assigned port addresses, which are separate from the memory addresses. The microprocessor reads and writes data to these port addresses, which are then passed on to the corresponding I/O device. This method uses less memory space, but it is more complex and slower than memory-mapped I/O.

The type of I/O interface used depends on the specific requirements of the system and the devices being interfaced. In general, memory-mapped I/O is used for high-speed devices, while port-mapped I/O is used for low-speed devices.