Victoria University of Bangladesh
Name: Md. Ziaul Hoque "Sohel"
Student ID: 2221220031
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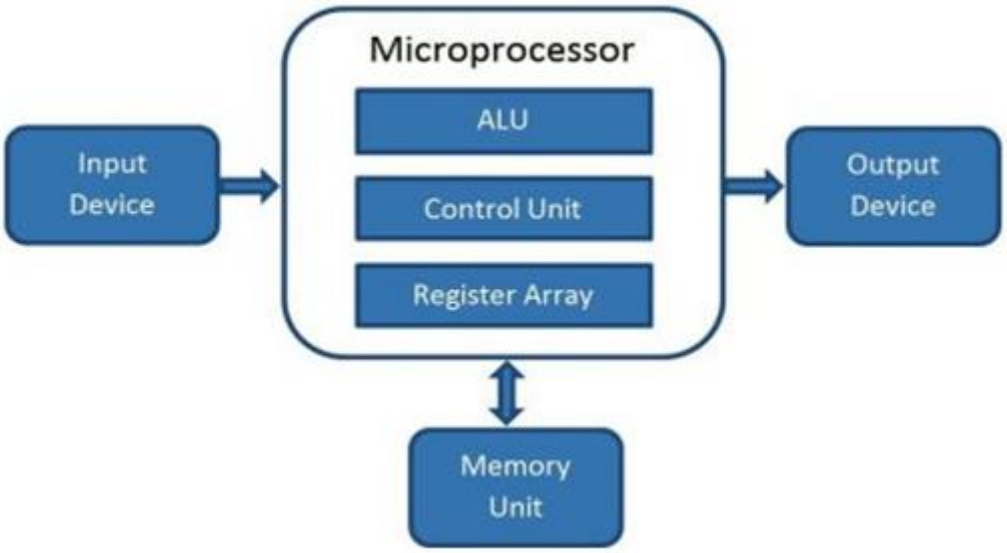
Answer to the Question No 1 (A)

Microprocessor:

Computer's Central Processing Unit (CPU) built on a single Integrated Circuit (IC) is called a microprocessor. A digital computer with one microprocessor which acts as a CPU is called microcomputer. It is a programmable, multipurpose, clock -driven, register-based electronic device that reads binary instructions from a storage device called memory, accepts binary data as input and processes data according to those instructions and provides results as output.

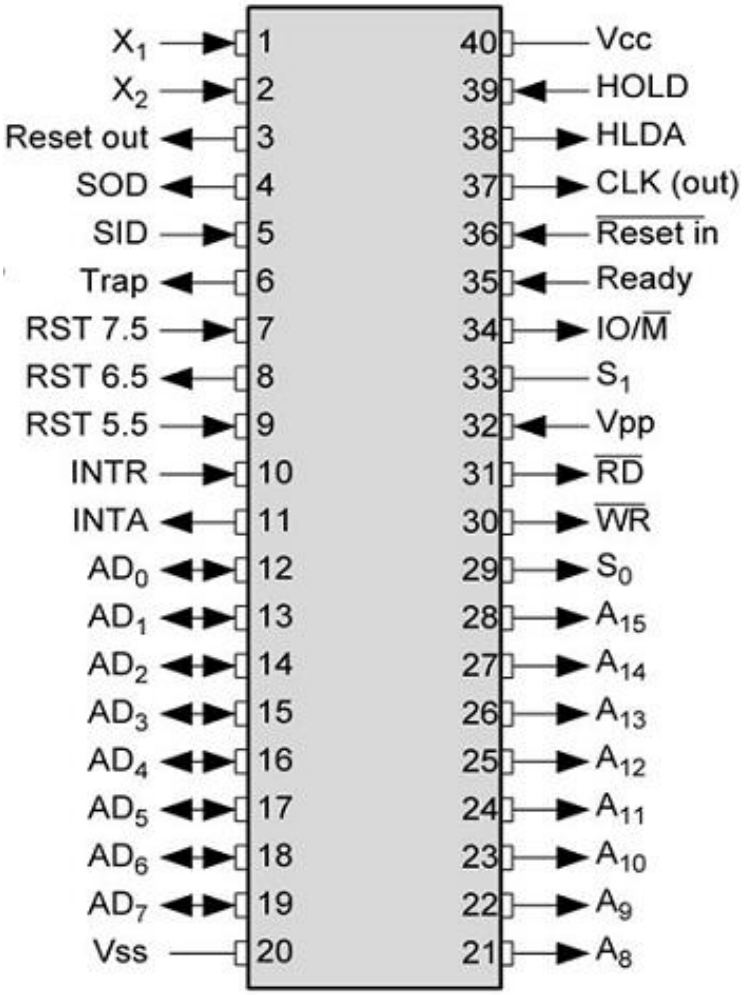
The microprocessor contains millions of tiny components like transistors, registers, and diodes that work together.

A microprocessor consists of an ALU, control unit and register array. Where ALU performs arithmetic and logical operations on the data received from an input device or memory. Control unit controls the instructions and flow of data within the computer. And, register array consists of registers identified by letters like B, C, D, E, H, L, and accumulator.



Answer to the Question No 1 (B)

The following image depicts the pin diagram of 8085 Microprocessor: –



The pins of an 8085 microprocessor can be classified into seven groups –

Address bus: A15-A8, it carries the most significant 8-bits of memory/IO address.

Data bus: AD7-AD0, it carries the least significant 8-bit address and data bus.

Control and status signals: These signals are used to identify the nature of operation. There are 3 control signal and 3 status signals. Three control signals are RD, WR & ALE.

RD: – This signal indicates that the selected IO or memory device is to be read and is ready for accepting data available on the data bus.

WR: – This signal indicates that the data on the data bus is to be written into a selected memory or IO location.
ALE :– It is a positive going pulse generated when a new operation is started by the microprocessor. When the pulse goes high, it indicates address. When the pulse goes down it indicates data.

Three status signals are IO/M, S0 & S1.

IO/M: - This signal is used to differentiate between IO and Memory operations, i.e. when it is high indicates IO operation and when it is low then it indicates memory operation.

S1 & S0:- These signals are used to identify the type of current operation.

Power supply: -There are 2 power supply signals – VCC & VSS. VCC indicates +5v power supply and VSS indicates ground signal.

Clock signals: -There are 3 clock signals, i.e. X1, X2, CLK OUT.

X1, X2: – A crystal (RC, LC N/W) is connected at these two pins and is used to set frequency of the internal clock generator. This frequency is internally divided by 2.

CLK OUT: – This signal is used as the system clock for devices connected with the microprocessor.

Interrupts & externally initiated signals: -Interrupts are the signals generated by external devices to request the microprocessor to perform a task. There are 5 interrupt signals, i.e., TRAP, RST 7.5, RST 6.5, RST 5.5, and INTR. We will discuss interrupts in detail in interrupts section.

INTA: – It is an interrupt acknowledgment signal.

RESET IN: –This signal is used to reset the microprocessor by setting the program counter to zero.

RESET OUT: –This signal is used to reset all the connected devices when the microprocessor is reset.

READY: – This signal indicates that the device is ready to send or receive data. If READY is low, then the CPU has to wait for READY to go high.

HOLD: – This signal indicates that another master is requesting the use of the address and data buses.

HLDA (HOLD Acknowledge): – It indicates that the CPU has received the HOLD request and it will relinquish the bus in the next clock cycle. HLDA is set to low after the HOLD signal is removed.

Serial I/O signals:
There are 2 serial signals, i.e. SID and SOD and these signals are used for serial communication.

SOD (Serial output data line) :– The output SOD is set/reset as specified by the SIM instruction.

SID (Serial input data line) :– The data on this line is loaded into accumulator whenever a RIM instruction is executed.

Answer to the Question No 1 (C)

Microprocessor classification :

Microprocessor is known as the computer processor. The IC or integrated Circuit makes the microprocessor. that is the brain of the computer machine. The microprocessor is known as the Processor or CPU (critical Processing Unit). all of the processors are brought about in a single tiny chip. The microprocessor decodes the statistics and tactics the facts. The processor's input has come from the reminiscence, which methods the enter to supply the preferred output. The microprocessor performs 3 tasks at some point of the processing of the data. Microprocessors are specifically three types, and their names are CISC, RISC and EPIC.

CISC Processor: The whole call of the CISC processor is complex guidance Set computer. with the aid of the name, it is regarded that the training set is complicated. complex instruction method a single training can keep many low-level commands. Loading statistics from memory or storing records inside the reminiscence is a basic example of complicated instructions. This CISC processor is used to limit the quantity of instructions in step with application. This processor needs a small size of RAM (Random get entry to memory). We use a few registers if a couple of operations require simplest a single preparation. The compiler works too little to assemble the facts from excessive-level to low-degree language or system language because the length of the CISC processor code is concise.
instance of CISC processor is Intel 386, Intel 486, Pentium, Pentium II, Pentium seasoned, IBM 370, IBM 268, VAX eleven/780 and many others.

RISC Processor: The whole name of the RISC processor is the decreased instruction Set pc. by way of the name, its miles recognized that the instruction is pretty easy and completed fast. The RISC processor's instructions get finished by simplest one clock cycle. This preparation also used some addressing modes. The RISC processor is used multiple registers, so the interaction with reminiscence is drastically much less. Example of CISC processor is IBM RS6000, DEC Alpha 21064, DEC Alpha 21164, DEC Alpha 210642, DEC Alpha 211066, DEC Alpha 211066, DEC Alpha 21068, DEC Alpha 21164, electricity pc 601, strength pc 604, power laptop 615, power computer 620, HP 7100LC and so on.

EPIC Processor: The overall name of the EPIC processor is Explicitly Parallel education Computing. by the name, it is recognized that the guidance works parallelly by way of the use of a compiler. This guidance works very complexly. a few clocks frequencies procedure the complex instruction of the EPIC processor. EPIC processor can encode the training. Furthermore, this processor can encode 128-bit bundles of guidance. every bundle consists of 3 complete commands in the set of 128-bit bundles. each of the three commands encoded in 41 bits is likewise a template 5-bit training. The five-bit template practice of the EPIC processor consists of the kind of the facts and also knows which preparation can be processed parallel. The EPIC processors include Intel structure-sixty-four or IA-64 HP-UX, 64-bit windows, undertaking Monterey, Novell Modesto, and many others. The Intel architecture-sixty-four is the first 64-bit microarchitecture based totally at the EPIC processor.

Answer to the Question No 2 (A)

DMA Operations:

Following is the sequence of operations performed by a DMA –

- Initially, when any device has to send data between the device and the memory, the device has to send DMA request (DRQ) to DMA controller.
- The DMA controller sends Hold request (HRQ) to the CPU and waits for the CPU to assert the HLDA.
- Then the microprocessor tri-states all the data bus, address bus, and control bus. The CPU leaves the control over bus and acknowledges the HOLD request through HLDA signal.
- Now the CPU is in HOLD state and the DMA controller has to manage the operations over buses between the CPU, memory, and I/O devices.

Answer to the Question No 2 (B)

8257 Pin Diagram:

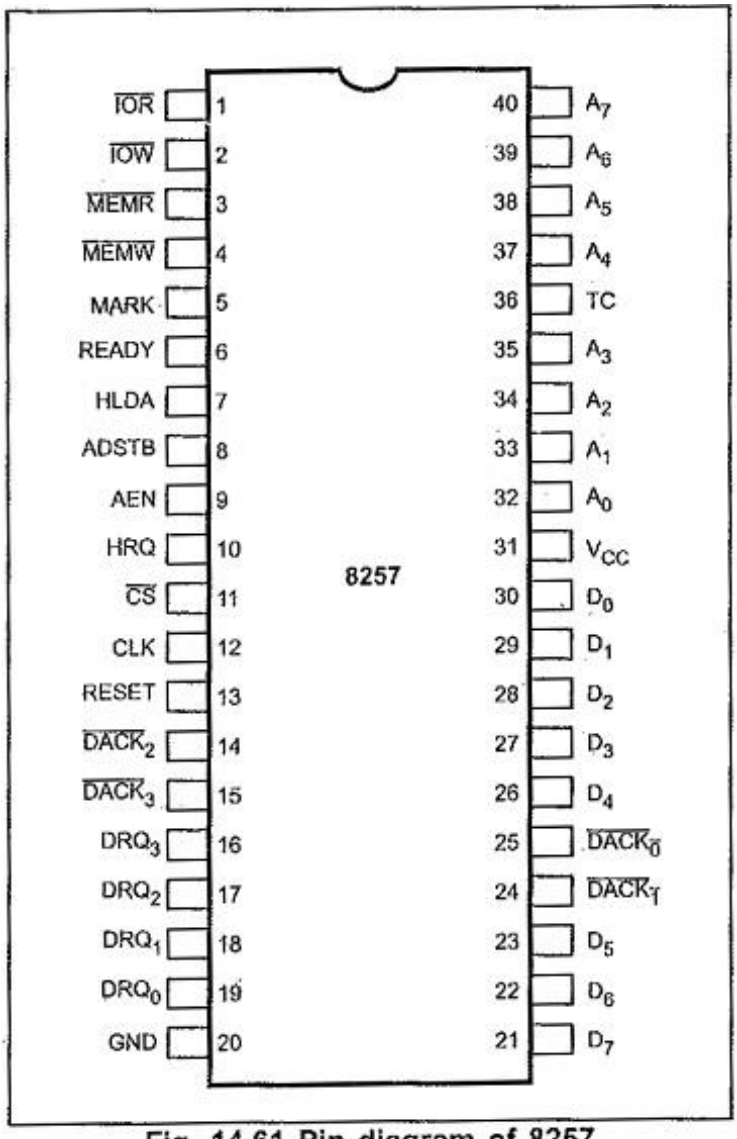


Fig. 14.61 Pin diagram of 8257

8257 Pin Description:

Address Bus (A_0-A_3 and A_4-A_7): The four least significant lines A_0-A_3 are bi – directional tri – state signals. In the idle cycle they are inputs and used by the CPU to address the register to be loaded or read. In the Active cycle they output the lower 4 bits of the address for DMA operation. A_4-A_7 are unidirectional lines, provide 4-bits of address during DMA service.

Address Strobe (ADSTB): This signal is used to demultiplex higher byte address and data using external latch.

Address Enable (AEN): This active high signal enables the 8-bit latch containing the upper 8-address bits onto the system address bus. AEN can also be used to disable other system bus drivers during DMA transfers.

Memory Read and Memory Write (MEMR, MEMW): These are active low tri-state signals. The MEMR signal used to access data from the addressed memory location during a DMA read or memory-to-memory transfer and MEMW signal is used to write data to the addressed memory location during DMA write or memory to memory transfer.

I/O Read and I/O Write (IOR and IOW): These are active low bi-directional signals. In idle cycle, these are an input control signals used by CPU to read/write the control registers. In the active cycle IOR signal is used to access data from a peripheral and IOW signal is used to send data to the peripheral.

Chip Select (CS): This is an active low input, used to select the 8257 as an I/O device during the idle cycle. This allows CPU to communicate with 8257 Pin Diagram.

Reset: This active high signal clears, the command, status, request and temporary registers. It also clears the first/last flip-flop and sets the Master Register. After reset the device is in the idle cycle.

Ready: This input is used to extend the memory read and write signals from the 8257 to interface slow memories or I/O devices.

Hold request (HRQ): Any valid DREQ causes 8257 to issue the HRQ. It is used for requesting CPU to get the control of system bus.

Hold Ackmiwledge (HLDA): The active high Hold Acknowledge from the CPU indicates that it has relinquished control of the system bus.

$DREQ_0$-$DREQ_3$: These are DMA request lines, which are activated to obtain DMA service, until the corresponding DACK signal goes active.

$DACK_0$-$DACK_3$: These are used to indicate peripheral devices that the DMA request is granted.

Terminal Count (TC): This is active high signal concern with the completion of DMA service. The TC output signal is activated at the end of DMA service, i.e. when present cycle is a last cycle for the current data block.

MARK: This output notifies the selected peripheral that the current DMA cycle is the 128^{th} cycle since the previous MARK output. MARK always occurs at 128 (all multiplies of 128) cycles from the end of the data block.

Answer to the Question No 3 (A)

Instruction Set in 8086 Microprocessor:

Rotate Instructions:

The following instructions come under this category:

Instruction	Description
RCL	Rotate all bits of the operand left by specified number of bits through carry flag.
RCR	Rotate all bits of the operand right by specified number of bits through carry flag.
ROL	Rotate all bits of the operand left by specified number of bits.
ROR	Rotate all bits of the operand right by specified number of bits.

Shift Instructions:

The following instructions come under this category:

Instruction	Description
SAL or SHL	Shifts each bit of operand left by specified number of bits and put zero in LSB position.
SAR	Shift each bit of any operand right by specified number of bits. Copy old MSB into new MSB.
SHR	Shift each bit of operand right by specified number of bits and put zero in MSB position.

Branch Instructions:

It is also called program execution transfer instruction. Instructions of this group transfer program execution from the normal sequence of instructions to the specified destination or target.

The following instructions come under this category:

Instruction	Description
JA or JNBE	Jump if above, not below, or equal i.e. when CF and ZF = 0
JAE/JNB/JNC	Jump if above, not below, equal or no carry i.e. when CF = 0
JB/JNAE/JC	Jump if below, not above, equal or carry i.e. when CF = 0
JBE/JNA	Jump if below, not above, or equal i.e. when CF and ZF = 1
JCXZ	Jump if CX register = 0

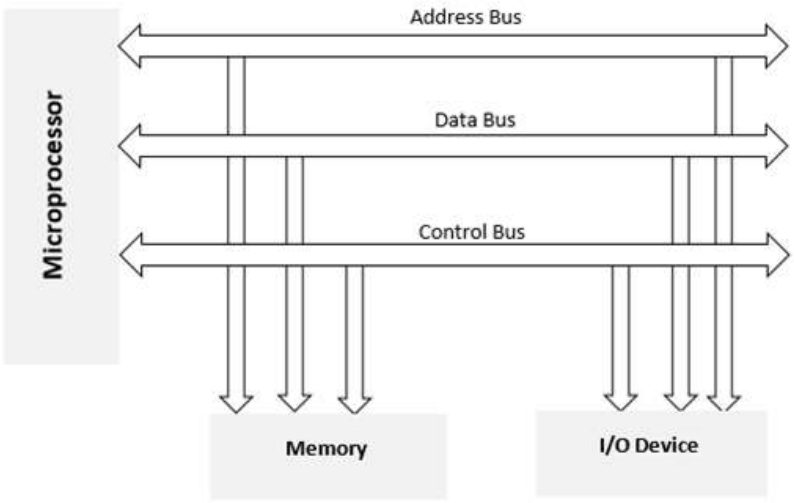
JE/JZ	Jump if zero or equal i.e. when ZF = 1
JG/JNLE	Jump if greater, not less or equal i.e. when ZF = 0 and CF = OF
JGE/JNL	Jump if greater, not less or equal i.e. when SF = OF
JL/JNGE	Jump if less, not greater than or equal i.e. when SF ≠ OF
JLE/JNG	Jump if less, equal or not greater i.e. when ZF = 1 and SF ≠ OF
JMP	Causes the program execution to jump unconditionally to the memory address or label given in the instruction.
CALL	Calls a procedure whose address is given in the instruction and saves their return address to the stack.
RET	Returns program execution from a procedure (subroutine) to the next instruction or main program.
IRET	Returns program execution from an interrupt service procedure (subroutine) to the main program.
INT	Used to generate software interrupt at the desired point in a program.
INTO	Software interrupts to indicate overflow after arithmetic operation.
LOOP	Jump to defined label until CX = 0.
LOOPZ/LOOPE	Decrement CX register and jump if CX ≠ 0 and ZF = 1.
LOOPNZ/LOOPNE	Decrement CX register and jump if CX ≠ 0 and ZF = 0.

Here, CF = Carry Flag
ZF = Zero Flag
OF = Overflow Flag
SF = Sign Flag
CX = Register

Answer to the Question No 3 (B)

Memory and I/O Interfacing:

Several memory chips and I/O devices are connected to a microprocessor.
The following figure shows a schematic diagram to interface memory chips and I/O devices to a microprocessor.



Memory Interfacing:

When we are executing any instruction, the address of memory location or an I/O device is sent out by the microprocessor. The corresponding memory chip or I/O device is selected by a decoding circuit. Memory requires some signals to read from and write to registers and microprocessor transmits some signals for reading or writing data.
The interfacing process includes matching the memory requirements with the microprocessor signals. Therefore, the interfacing circuit should be designed in such a way that it matches the memory signal requirements with the microprocessor's signals.

I/O interfacing:

As we know, keyboard and displays are used as communication channel with outside world. Therefore, it is necessary that we interface keyboard and displays with the microprocessor. This is called I/O interfacing. For this type of interfacing, we use latches and buffers for interfacing the keyboards and displays with the microprocessor.
But the main drawback of this interfacing is that the microprocessor can perform only one function.

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