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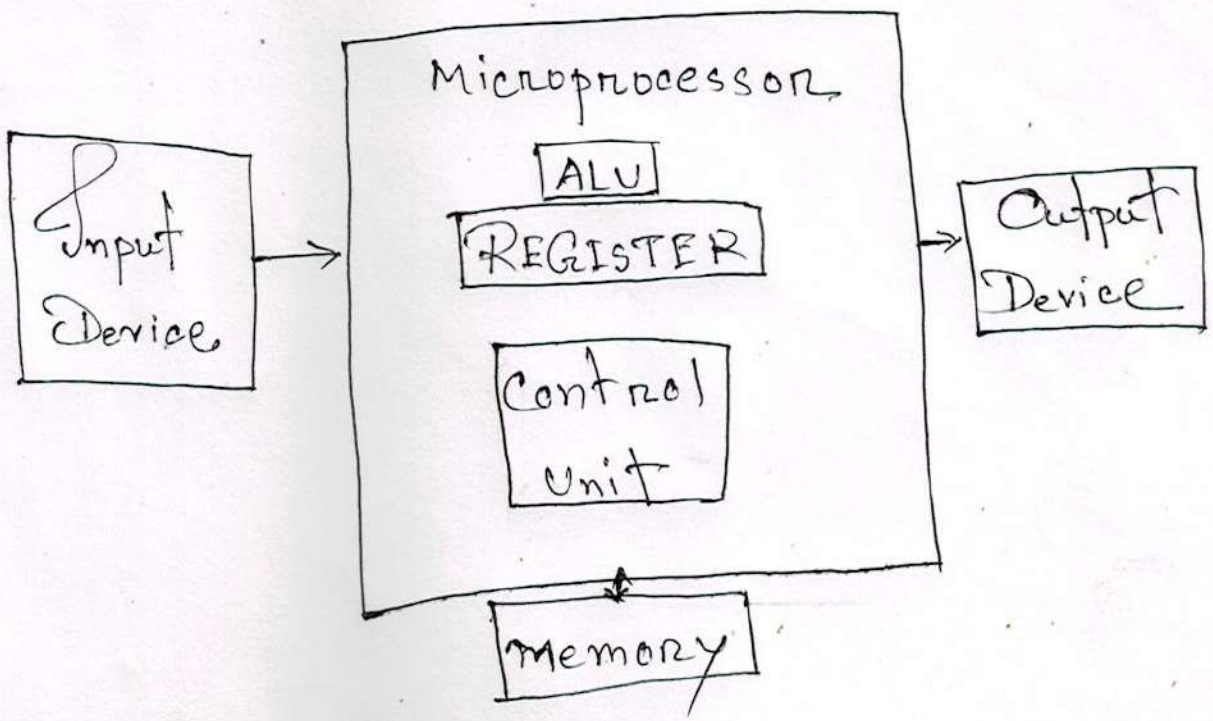
Course code: CSE 413

Ans to the Q.NO: 01 - (a)

(a)
Ans: **Microcomputer**: A digital computer with one microprocessor which acts as a cpu is called microcomputer. Computer's central processing unit (CPU) build on a single Integrated circuit is called microprocessor.



Blog Diagram of Besic Microcomputer.

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* Features of Microprocessor: Features of Microprocessor are given below:

1. Architecture: Microprocessors are availabe in 8 bit, 16 bit, 32 bit, 64 bit architectures. This bit size indicates the size of the data, the processor can handle and the scope of the memory the processor can adress during it's operation. The bit sizes can also be called buswidth.

As the processor width increases programme code size comes down. Though it largely challenging to code in 64 bit processor than 8 bit, the external tool, aides, Integrated development environment make it easier to develop programmes in computers with higher to develop programme width processor. Due to this labour cost also is lower.

2. Parallel processing: The multicore chip that contains more than one processor in it, enables parallel processing of independent portions of a task. It reduces the overall time taken to improves efficiency, Data indensive jobs will be processed in this mode by data scintists.

3. Multiprocessing and time sharing:

The time is divided into several equal slices and it is allolled to various processes into a round-ndein fashion.

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As the available cpu is only one in the system and that cpu will process that allotted process for that slice of time or till the interrupt occurs whichever is earlier. The computer resource is shared accross multiple process running concurrently.

4. Categories of Microprocessor:

Based in the way instruction set is constructed and how they getting executed, microprocessors are categorised into -

(a) Reduced Instruction set computer (RISC)
(b) Complex Instruction set computer (CISC)
(c) Special Purpose Processors.

5. Size-cost: As a technology improves the cost either comes down or the values for the money increases. The user gets more features for the same money or a slightly higher amount spent.

6. Power consumption: Microprocessor consume less power due to their material content and technology used in manufacturing.

7. versatility: Microprocessors can be deployed for multiple purpose by simply configuring the sofwere in them.

8. Reliability: Microprocessors are highly reliable in their operation and their performance is steady even under complex conditions.

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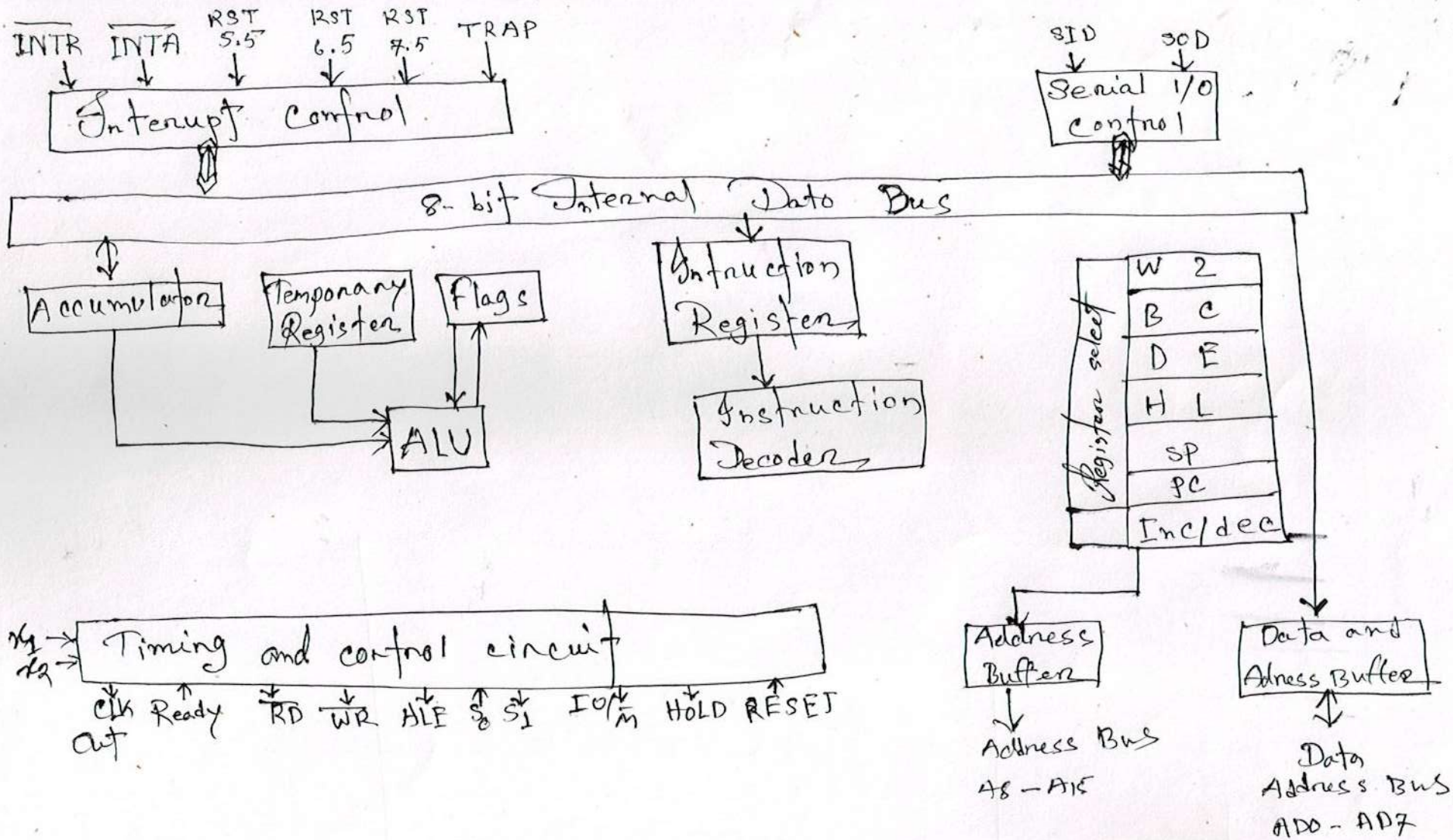

Fig: Architecture of 8085 Microprocessor.

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Ans: Bit manipulation instruction: Bit manipulation instruction sets are extensions to the x86 instruction set architecture for microprocessors from Intel and AMD.

The purpose of these instruction sets is to improve the speed of bit manipulation. All the instructions in these sets are non-SIMD and operate only on general-purpose registers.

There are two sets published by Intel: BMI and BMI2. They were both introduced with the Haswell micro-architecture with BMI1 matching features offered by AMD's ABM instruction set and BMI2 extending them. Another two sets were published by AMD: ABM and TBM.

Bit manipulation is the act of algorithmically manipulation bits or other pieces of data shorter than a word. Computer programming tasks that require bit manipulation include low-level device, control, error detection and correction algorithms, data compression, encryption algorithms and optimization. For most other tasks, modern programming languages allow the programmer to work directly with abstractions instead of bits that represent those abstractions. Source code that does bit manipulation makes use of the bitwise operations: AND, OR, XOR, NOT, and possibly other operations analogous to the boolean operations; these are also bit shifts and operation-

1.c

- to count Ones and Zeros, find high and low One or Zero, Set reset and test bits, extract and insert fields, mask and zero fields, gather and scatter bits to and from specified bit positions or fields.

Bit manipulation, in some cases, can obviate or reduce the need to loop over a data structure and can give many-fold Speed ups, as bit manipulations are processed in parallel.

~~Ans: to the Q.NO: 2 (a)~~

(a) Ans: How DMA operations are performed:

Initially, when any device has to Send data between the device and the memory, the device has to Send DMA request (DRQ) to DMA Controller.

The DMA Controller sends Hold request to the cpu and waits for the cpu to assert the HLDA.

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(b) 8257 pin discription:

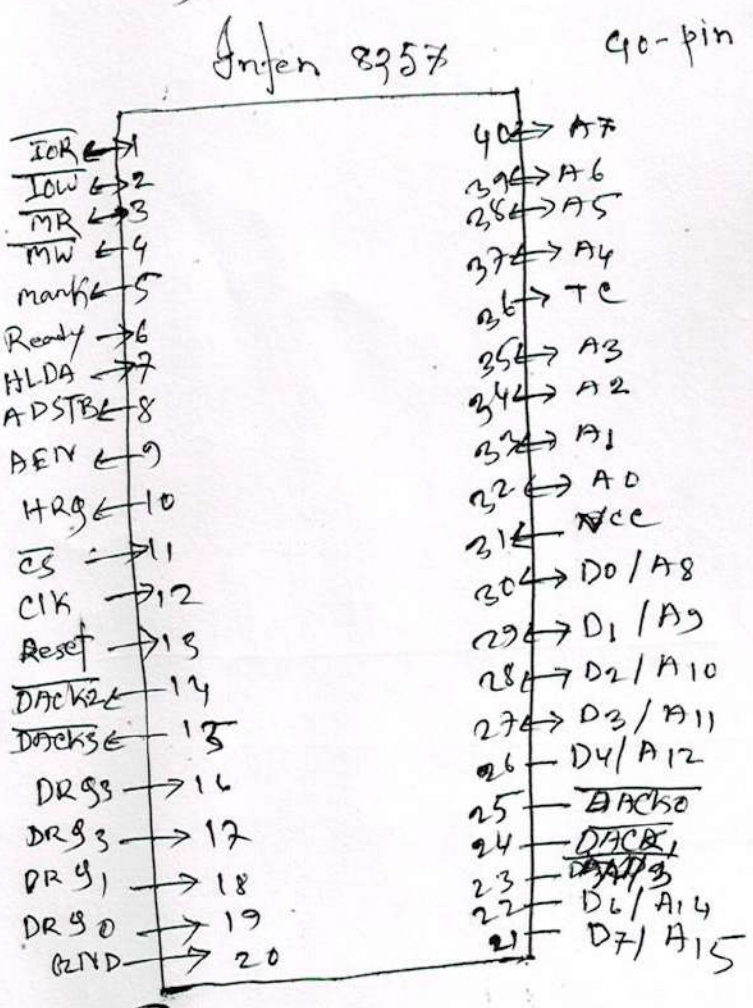

Fig: physical pin diagram of Intel 8257.

Description: D7-D0 / A15-8: for communicating with the processor there are 8 bidirectional data pins. When the processor is in active and the 8257 active state it is in slave mode, when the processor remains in the HOLD state and 8257 behaves as the master, they are used to send out the most significal 8 bits of memory adress.

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A3-0 : When the processor remains in active state and are used as address oput pins and are used as address input pins of 8257. Hence to select one of the registers inside the 8257 the pins are used.

A3-0	Selected Register
0000	AR0
0001	CR0
0010	AR1
0011	CR1
0100	AR2
0101	CR2
0110	AR3
0111	CR3
1000	Control Status
1001 to 1111	Unused

RESET: Reset is the active high input pin which is connected to the Reset Outpin of 8085. After 8257 is reset, the control register contents to 00H.

DR3-3-0: These pins active high DMA request input pins, assigned to one for each DMA channel. These are activated by some special purpose I/O port chips like Intel 8257 floppy disk controller, and Intel 8275 CRT controller. In fixed priority mode DR0 has the highest and DR3 the lowest priority.

DACK 3-0 : These are the active low DMA acknoledge out put pins, only for one for every four DMA channels, Intel 8275.

IOR*: It is an active low input pin which is activated by the processor to read an Address register, counter register when 8257 works in the slave mode.

IOW*: It is an active low input pin which is activated by the processor to write to an address register, counter register when the 8257 remains in the slave mode.

MR*: It is an active low output pin which operates tristate when 8257 is in the slave mode.

MW*: It is also an active low output pin which is in tristate when 8257 is in the slave mode.

CS*: Unlike others it is also an active low input pin for selecting chip.

CLK: It is the input pin of the clock. The maximum allowed frequency for this clock is about 3MHz. The input of the clock is connected to the output of 8085 in a system which is based on 8085.

Ready: Ready is an active high input pin which is an active function line the ready input of 8085.

HRQ: HRQ is for hold request which is an active high Output pin also connected to the hold input of 8085.

HLDA: HLDA means Hold acknoledge which output is 8085.

TC: TC means terminal count which is an high output pin.

MARK: This is also high output Pin which is activated when the least significant 7 bits of the control register become 0 for the DMA channel which is getting serviced.

AEN: AEN stands for address enable. It is an active high output pin performing the same function as output of 8085.

ADSTB: ADSTB signifies address strobe which is an active high output pin performing the same function as output of 8085. In Intel 825x, if there is output on this pin as 0. If it is in the slave mode.

Ans: to the Q: NO: 03 (a)

Rotate instruction: The following instruction came under this category :-

Instruction	Description
RCL	Rotate all bits of the operand left by specified number of bits through carry flag.
RCR	Rotate all bits of the operand right by specified number of bits through carry flag.
ROL	Rotate all bits of the operand left by specified number of bits.
ROR	Rotate all bits of the operand right by specified number of bits.

Shift Instruction: The following instructions came under this category :-

Instruction	Description
SAL or SHL	Shift each bits of operand left by specified number of bits and put zero in LSB position.
SAR	Shift each bit of any operad right by specified number of bits. Copy old MSB into new MSB.
SHR	Shift each bit of operand right by specified number of bits and put zero in MSB position.

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Branch Instruction: The following instructions come under this category:-

Instruction	Description
JA or JNBE	Jump if above, not below, or equal i.e. when CF and ZF = 0
JNE/JNB/JNC	Jump if above, not below, equal or not carry i.e when CF = 0
JB/JNAE/JC	Jump if below, not above, or equal i.e when CF ~~and ZF = 0~~
JCXZ	Jump if CX register = 0
JBE/JNA	Jump if below, not above, or equal ie. when CF and ZF = 1
JE/JZ	Jump if 0 or equal i.e when ZF = 1
JG/JNLE	Jump if greater, not less or equal i.e when ZF = 0 & CF = OF
JGE/JNL	Jump if greater, not less or equal i.e when SF = OF
JL/JNGE	Jump if not greator if less than or equal i.e when SF ≠ OF
JLE/JNG	Jump if less, equal or not greater i.e when ZF = 1 & SF ≠ OF
JMP	Causes the program execution to jump unconditionally to the memory adress or label given in the instruction.
CALL	Calls a procedure whose address is given in the instruction and saves their return address to the stack.
RET	Returns program excution from a procedure to the next instruction or main program.
IRET	Returns program execution from an interrupt service procedure to the main program

INT	used to generate software interrupt at the desired point in a program.
INTO	software interrupts to indicate overflow after arithmetic operation.
LOOP	Jump to defined label until cx = 0
LOOPZ/LOOPE	Decrement CX register and jump if CX≠0 and ZF = 1
LOOPNZ/LOOPNE	Decrement cx register and jump if CX≠0 and ZF = 0

Here,

cf = Carry Flag

ZF = Zero Flag

OF = Overflow Flag

SF = Sign Flag

cx = Register.

Ans: the 1 of 1NO: 03 (b)

Memory interfacing: When we are executing any instruction, the address of memory location or an I/O device is sent out by the microprocessor. The corresponding memory chip or I/O device is selected by a decoding circuit. Memory requires some signals to read from and write to registers and microprocessor transmit some signals for reading or writing data. The interfacing process includes matching the memory requirments with the microprocessor signals. Therefore, the interfacing circuit should be designed in such a way what it matches the memory signal requirement with the microprocessor's signals.

I/O interfacing: As we know, keyboard and displays are used as communication channel with outside world. Therefore, it is necessary that we interface keyboards are displays with the microprocessor. This is called I/O interfacing for this type of interfacing, we used letches and buffers for interfacing the keyboards and displays with the microprocessor. But the main drawback of this interfacing is the microprocessor can perform only one function.