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Final- Assessment

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Ans to the QU:NO: 1

(1) B (a)

Below describe IBM z EC12 I/O channel subsystem structure :-

The CSS allows channel I/O operations to continue independently of other operations within the server. This function allows other functions to resume after an I/O operation is initiated.

channel :-

The communication path from the channel subsystem to the connected control units and I/O devices. The channel subsystem communicates with I/O devices by using channel paths between the channel subsystem and control units.

physical channel ID (PCHID) :-

A PCHID reflects the physical location of a channel-type interface. A PCHID number is based on the I/O drawer or cage location, the channel feature slot number, and the port number of the channel feature.

A CHPID does not directly correspond to a hardware channel port, but is assigned to a PCHID in Hardware configuration definition (HCD) or input/output configuration program (IOCP).

subchannel :-

provides the logical appearance of a device to the program, and contains the information that is required for sustaining a single I/O operation. A subchannel is assigned for each device that is defined to the logical partition.

Input/output (I/O) device :-

provides external storage, which is a means of communication between data processing system, or a means of communication between a system and its environment. In the simplest case, an I/O device is attached to one control unit and is accessible through one channel path.

① (b)

I/O Hardware is a set of specialized hardware devices that help the operating system access disk drives, printers, and other peripherals. These devices are located inside the mother board and connected to the processor using a bus. They often have specialized controllers that allow them to quickly respond to requests from software running on top of them or even respond directly to commands from an application program. This post will discuss in detail I/O Hardware basics such as daisy chain expansion bus controller memory-mapped I/O Direct Memory Access (DMA). The daisy chain, expansion bus, controller, and host adapter are used to access the I/O hardware. The daisy chain is a method of connecting multiple I/O devices with each other through a single connection point (pin). Each device can be accessed by plugging into any of the pins on this connection point.

The expansion bus connets devices together in parallel with each other so that they can be accessed simultaneously by using only one cable insted of several cables (one per device). This design allows you to connect more than one peripheral device while maintaining compatibility with older systems that may not support additional peripherals or features such as memory-mapped I/O (MMIO). A controller manages all incoming data from its associated port and sends outgoing commands from its associted port, it's like an interface between an application software program and hardware components such as disk drives or network adaptes. A host adapter is a bridge between the system bus and the expansion bus. It allows you to connect multiple expansion cards at the same time and provides additional interfaces for those cards such as DMA or mmio.

A controller manages all incoming data from its associated port and sends outgoing commands from its associated port; it's like an interface between an application software program and hardware components such as disk drives or network adapters. I/O hardware is a collection of devices that are used to make it easier for the CPU and other processors on your computer to communicate with the outside world. These devices may include, peripheral controller cards (also called I/O adapters) connect to the expansions bus (sometimes called PCI or ISA) and control how data is transferred between different parts of a computer system. Interrupt request lines (IRQs) and serial ports, which allow multiple peripherals such as keyboards, mice, and printers to communicate with one another without having their own dedicated channel in memory.

(1)(c)

Below describe Three techniques for Input of a Block diagram:

Mainly computer system consists of three parts, that are central processing unit (CPU), Input devices, and output devices. The central processing unit (CPU) is divided into two parts again arithmetic logic unit (ALU) and the control unit (CU). The set of instruction is in the form of raw data. A large amount of data is stored in the computer memory with the help of primary and secondary storage devices. The CPU is like the heart/brain of the computer. The user does not get the desired output, without the necessary option taken by the CPU. The central processing unit (CPU) is responsible for the processing of all the instructions which are given by the user to the computer system.

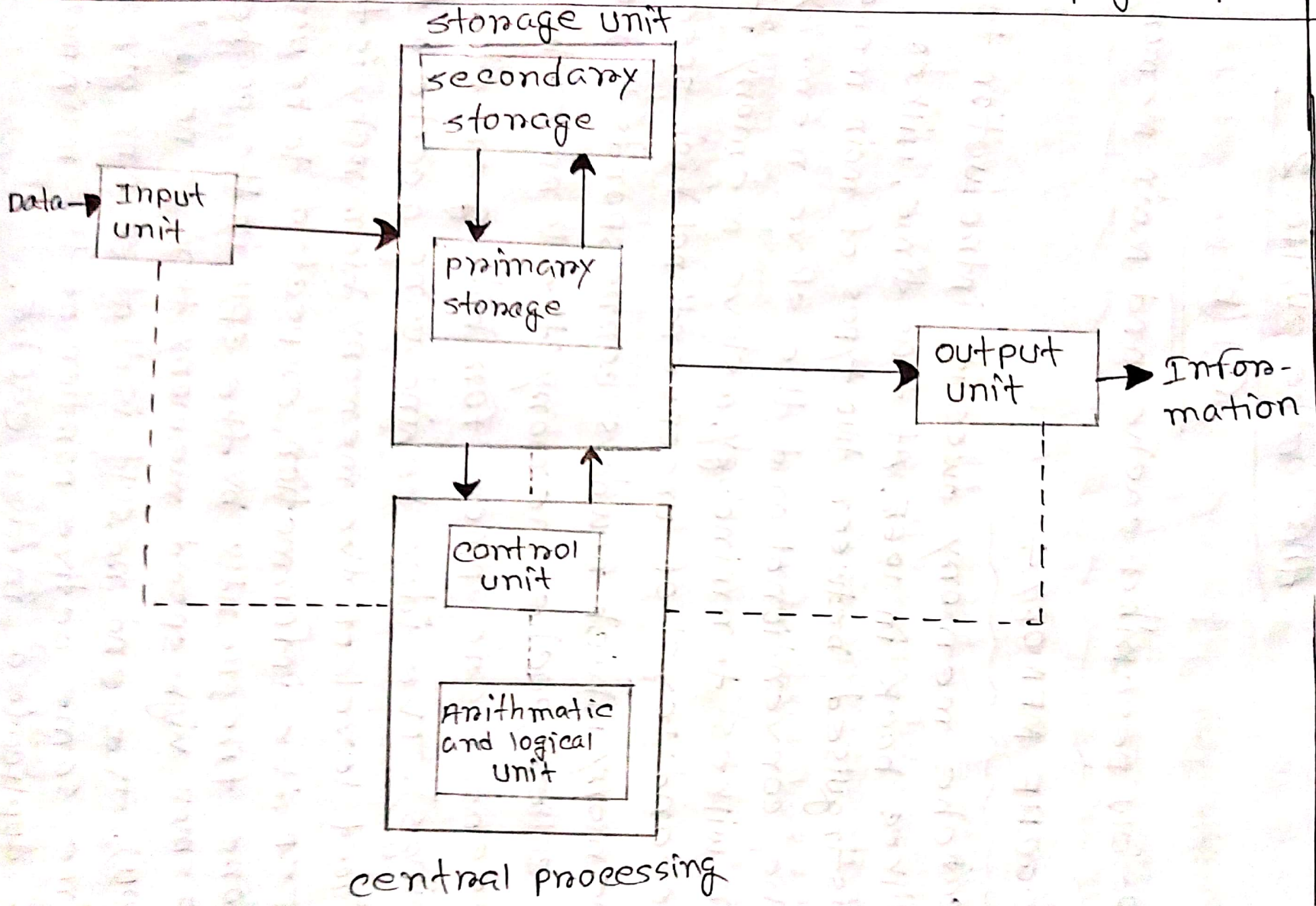

Fig: Block Diagram of the computer

Ans to the qu. No: 2

(2) (b)

Below describe cache and main memory:-

CACHE MEMORY :-

cache memory owes its introduction to wilkes back in 1965. At that time, wilkes distinguised between two types of main memory. The conventional and the slave memory. In wilkes terminology, a slave memory is a second level of unconventional high-speed memory, which nowdays corresponds to what is called cache memory (the term cache means a safe place for hiding or storing things). The idea behind using a cache as the first level of the memory hierarchy is to keep the information expected to be used more frequently by the cpu in the cache (a small high-speed memory that is near the cpu). The end result is that at any given time some active portion of the main memory is duplicated in the cache.

Main memory :-

The main memory is the fundamental storage unit in a computer system. It is associatively large and quick memory and saves programs and information during computer operations. The technology that makes the main memory work is based on semiconductor integrated circuits. RAM is the main memory. Integrated circuit Random Access Memory (RAM) chips are applicable in two possible operating modes are as follows :-

static :-

It consists of internal flip-flops, which store the binary information. The stored data remains solid considering power is provided to the unit. The static RAM is simple to use and has smaller read and write cycles

Dynamic :-

It saves the binary data in the structure of electric charges that are used to capacitors.

(2) (b)

Below describe Logical and physical caches with description:-

cache memory can be located either side of a memory management unit and uses either physical or logical addresses its tag data. In terms of performance, the location of the cache can dramatically affect system performance. with a logical cache, the tag information refers to the logical addresses currently in use by the executing task. If the task is switched out during a context switch, the cache tags are no longer valid and the cache, together with its often hard-won data must be flushed and cleared. The processor must now go to main memory to fetch the first instructions and wait until the second iteration before any benefit is obtained from the cache.

However, cache accesses do not need to go through the MMU and do not suffer from any associated delay.

physical caches use physical addresses, do not need flush-ing on a context switch and therefore data is preserved within the cache. The disadvantages is that all accesses must go through the memory management unit, thus incurring delays. particular care must also be exercised when pages are swapped to and from disk. If the processor does not invalidate any associated cache entries, the cache contents will be different from the main memory contents by virtue of the new page that has been swapped in. most internal caches are now designed to use the physical address (notable exceptions are some implementations of the SPARC architecture which use logical internal cache

Ans to the qu. No: 3

(3) (a)

Draw central processing unit :-

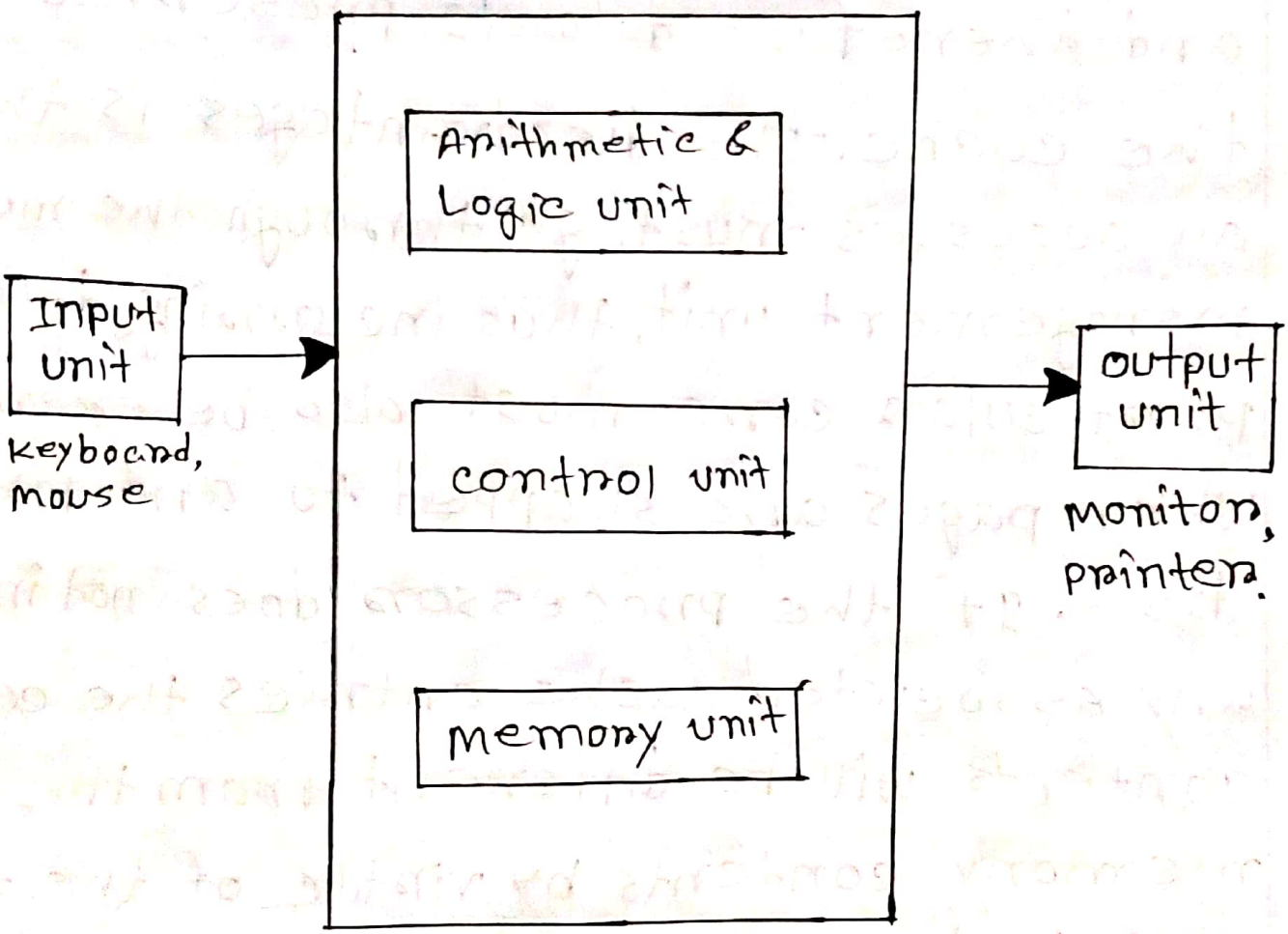

Fig. central processing unit (CPU).

main components and interactions with the main memory and I/O ÷

main memory ÷

The Random Access memory is the main memory of the computer system, which is known as RAM. The main memory can store the operating system software, application software, and other information. The RAM is one of the fastest memory, and it allows the data to be readable and writeable.

Input / output ÷

The computer system's I/O architecture is its interface to the outside world. This architecture is designed to provide a systematic means of controlling interaction with the outside world and to provide the operating system with the information it needs to manage I/O activity effectively.

③ (b)

An direct address is an absolute, relative, or symbolic address of a location that contains another address. An indirect address must be followed by one or more indirection-symbols to indicate a corresponding number of levels of indirect addressing. In this section, we discuss the assembly language features and use of the X86 family, we present the basic organizational features of the system, the basic programming model, the addressing modes, sample of the different instruction types used and finally examples showing how to use the assembly language of the system in programming sample real-life problems. In the late 1970s, Intel introduced the 8086 as its first 16-bit microprocessor. This processor has a 16 bit external bus.

The 8086 evolved into a series of faster and more powerful processors starting with the 80286 and ending with the pentium. The letter was introduced in 1993, this Intel family of processors is usually called the x86 family. The Intel pentium processor has about three million transistors and its computational power ranges between two and five times that of its predecessor processor the 80486. A number of new features were introduced in the pentium processor among which is the incorporation of a dual-pipelined superscalar architecture capable of processing more than one instruction per clock cycle. The basic programming model of the 386, 486, and the pentium.