Victoria University
OF
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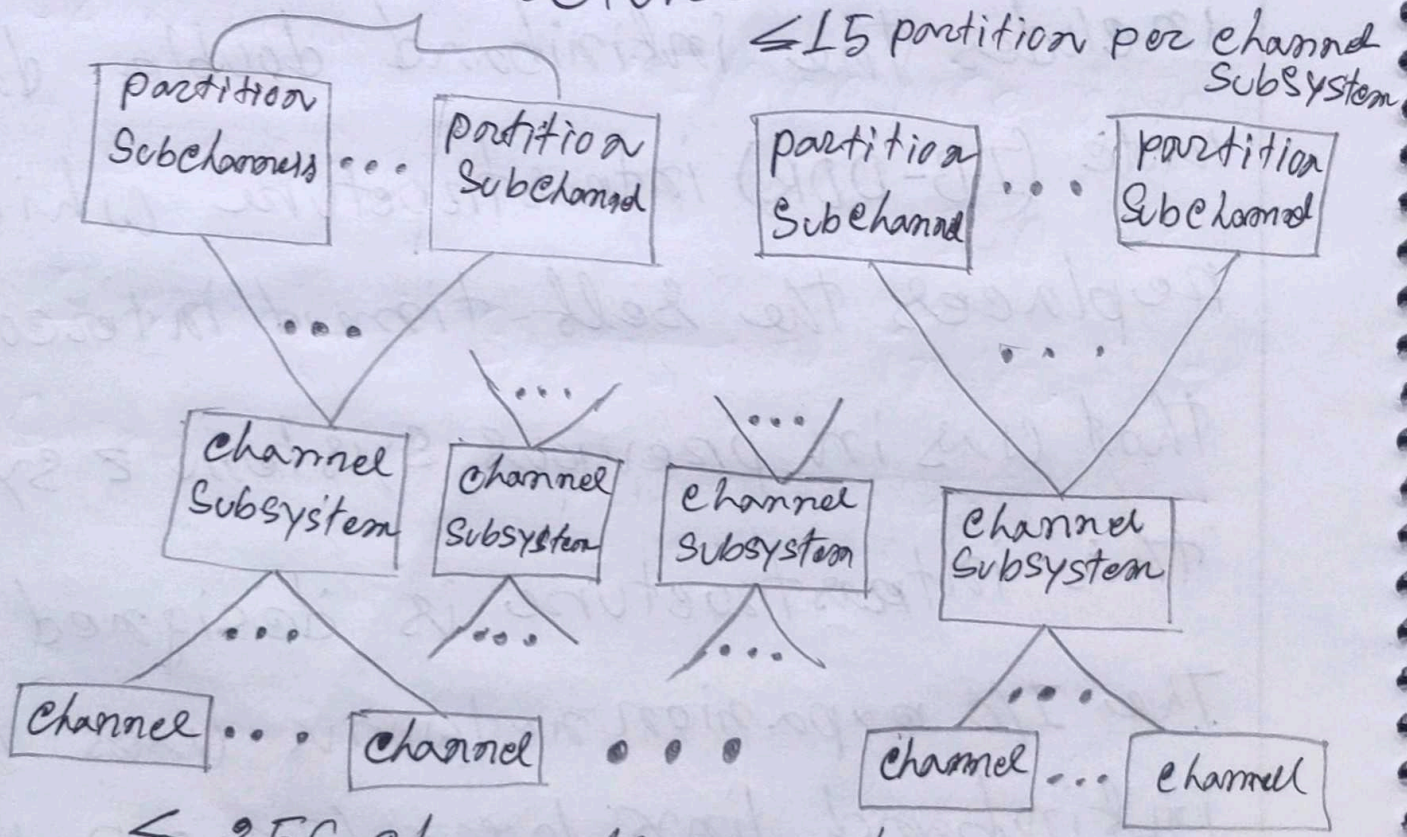
Ans to the Q. NO. 1(a)

The zEC12 I/O Subsystem is Similar to the one on Z196 and includes a PCIe infrastructure The I/O Subsystem is supported by both a PCIe bus and an I/O bus Similar to that of Z196. It includes the infiniband double date rate (IB-DDR) infrastructure which replaces the self-timed interconnect that was in previous system z systems this infrastructure is designed throughout The I/O expansion network uses the infiniband link layer (IB-2, Double Data Rate).

zEC12 offers three I/O infrastructure elements for holding the I/O features PCIe I/O drawers for PCIe features and I/O drawers and I/O cages for xor pele features.

Channel structure



IBM zEC12 I/O

Ans To The Q. NO. 2(b)

When an I/O device completes an I/O operation The Following Sequence of hardware events occurs

The device issues an interrupt Signal to The processor

The processor Finishes The execution of The current instruction before responding to the interrupt.

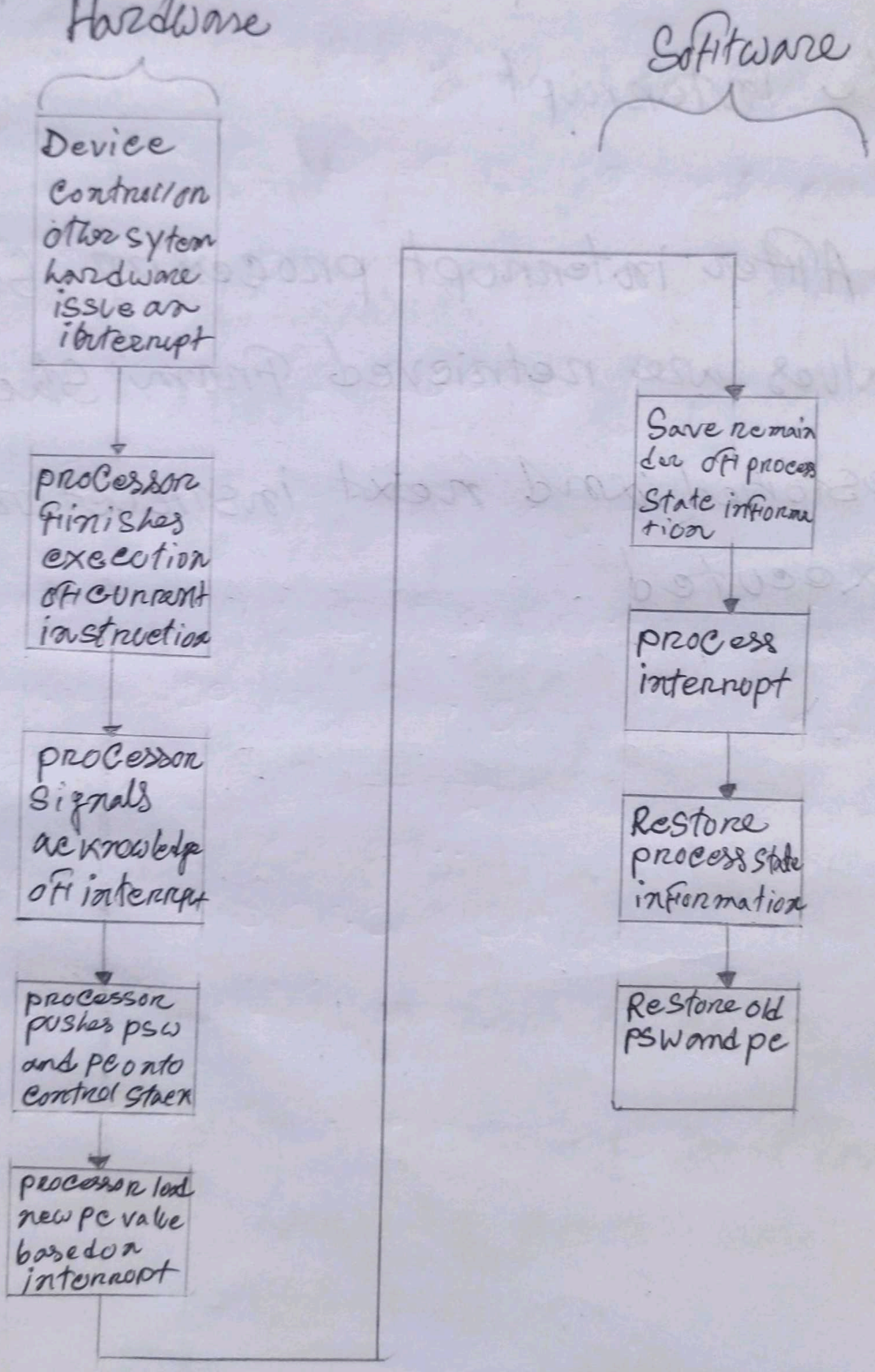
The processor test for an interrupt and Sends an acknowledgment Signal to the device That issued the interrupt.

The processor now needs to save information needed to resom the current program at the point of an interrupt. The minimum information saved to be is the status to the processon and locations of the status of the processon and location of the next instruction to be executed.

The processon now loads the program coonter with the entry location of interrupt handling program.

The interrupt handler next processes the interrupt

After interrupt processing, Saved register values are retrieved from Stack and restored and next instruction will be executed.


Hardware
Softwware
Device controller other system hardware issue an interrupt
processor finishes execution of current instruction
processor signals acknowledge of interrupt
processor pushes psw and pc onto control stack
processor load new pc value based on interrupt
Save remainder of process state information
process interrupt
Restore process state information
Restore old PSW and pc

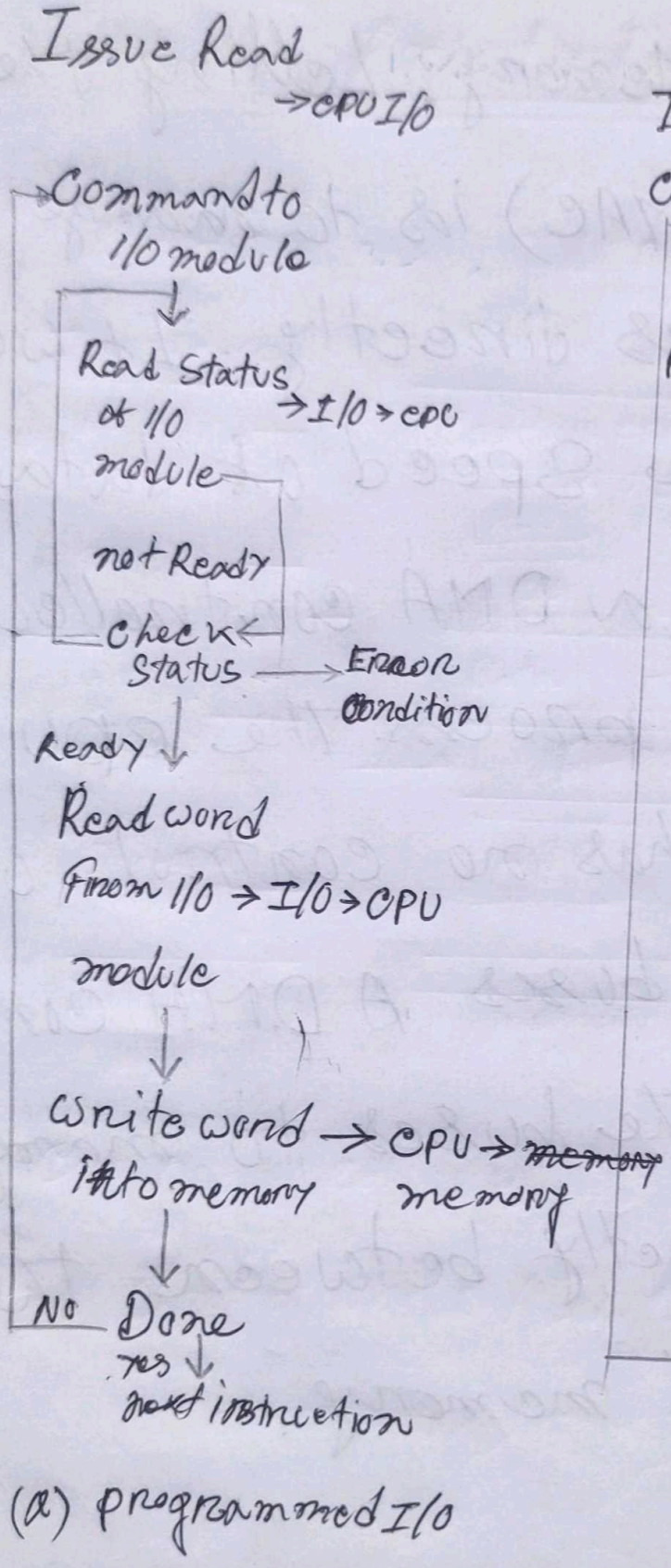
Ans to the Q.NO. 1(c)

Three techniques for Input of a Block diagram

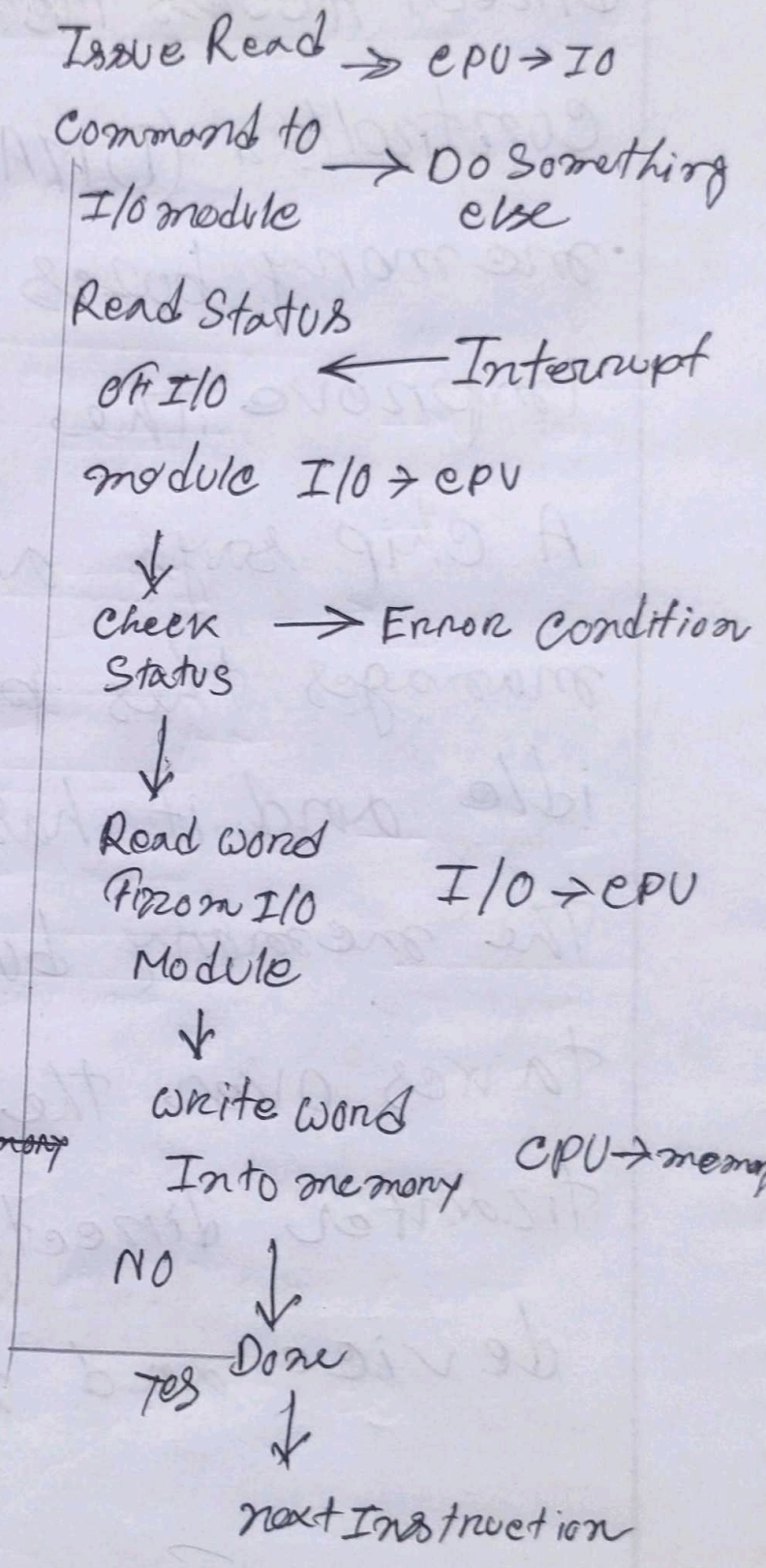
programmed I/O : In this method, The cpu stays in a program loop until The I/O unit indicates that is ready for data transfer. It is a time consuming process for the cpu. The programmed I/O method is particulary useful in Small low Speed computers. The cpu Sends the read command to the I/O device and waits in the program loop until it receive a response from the I/O device.

Interrupt I/O: The problem with programmed I/O is that the CPU has to wait for the ready signal from the I/O device. So alternative to this is interrupt I/O. In this method, the CPU issues a read command to the I/O device about the status. When the I/O device is ready it sends an interrupt signal to the processor.

Direct Access Memory: Letting the DMA controller (DMAC) is to manage the memory buses directly. It would improve the speed of data transfer. A chip says a DMA controller (DMAC) manages this process. The CPU is idle and it has no control over the memory buses. A DMA controller takes over the buses to manage the transfer directly between the I/O device and memory.



(a) programmed I/O



(b) Interrupt I/O

Issues Read CPU → DMA

block command → Do Somethings
To I/O module else

Read Status

OF DMA ← Interrupt
module DMA → CPU

↓

Next Instruction

(c) Direct memory access.

Ans to the Q. NO. 2(a)

In Computing, a cache is a high-speed data storage layer which stone a subset of data, typically transient in nature so that future request for that data are served up faster than is possible by accessing the data's primary storage location, Caching allows you to efficient reuse previously retrieved or computed data.

The data in a cache is generally stored in fast access hardware such as RAM (Random-access memory) and may

also be used in connection with a software component. A cache's primary purpose is to increase data retrieval performance by reducing the need to access the underlying slower storage layer.

Main memory is the primary, internal workspace in the computer, commonly known as RAM (Random access memory) specifications such as 4GB, 8GB, 12GB and 16GB almost always refer to the capacity of RAM.

In contrast, disk or Solid State Storage capacities in a computer are typically 128 GB or 256 GB and higher. In a Smart phone or tablet, Solid State Storage generally starts at 32 GB or 64 GB, The exception to these rules is the chromebook, which may have only 16 GB of Solid State Storage (see chromebook) See memory and Storage.

Ans to the Q. NO. 2(b)

A logical address is generated by CPU while a program is running Since a logical address does not physically exists it is also known as a virtual address. This address is used as a reference by the CPU to access the actual physical memory location.

There is a hardware device called memory management unit is used For mapping logical address to its

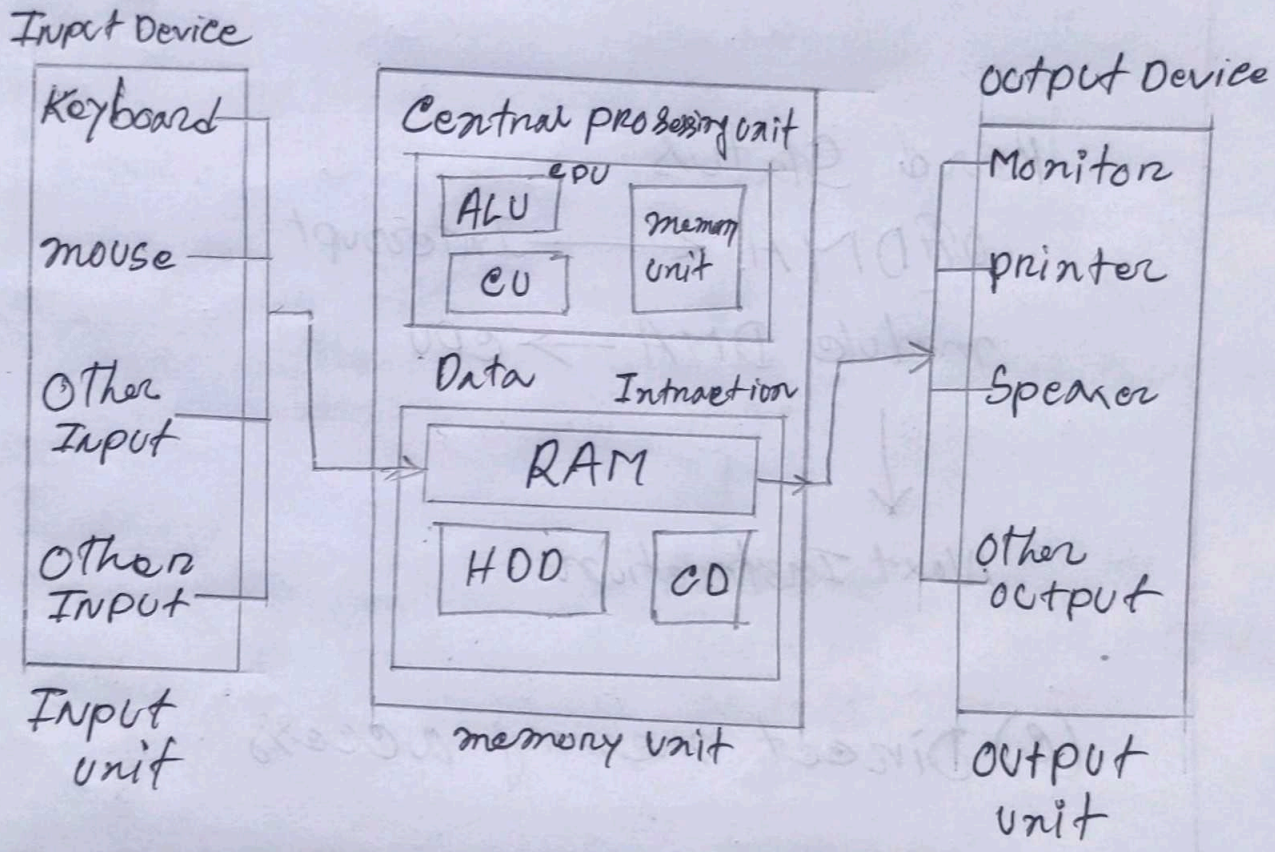
Corresponding physical address. A physical address identifies the physical location of a specific data element in memory The user never directly deals with the the physical address but can determine the. physical address

The user program generates the logical address and believes That the program is running in this logical address space but the program needs physical memory for its execution, therefore the logical address must be mapped

to the physical address by the MMU before the addresses are used for all physical address corresponding to the logical addresses in a logical address space.

Ans to The Q. NO- 3(a)

Computer System



Central processing units :-

Control unit : ALU, CU, Memory unit

Memory unit :- RAM, HDD, CD

Ans to the Q.NO-3(b)

Indirect addressing FOR x86

In register indirect addressing mode, the address of the memory location where, the operd resides is held by a register.

The register used FOR the propose are SI, DI and BX IF these three register are used as pointer they must be combined with DS in order to generate the 20 bit physical Address

processor register		
AX	AH	AL
BX	BH	BL
CX	CH	CL
DX	DH	DL
SI		
DI		
BP		
SD		
CS		
DS		
SS		
ES		

Memory	
memory Address	Data
10000	AAH
10001	BBH
10002	CCH
10003	EEH
10004	DDH
10005	EEH
10006	FFH
10007	IIH
10008	22H
10009	33H
10004	44H