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Program: B.Sc in (CSE)

Final Examination

Semester: Fall-2022

Batch: 22nd (Evening).

Course Code: CSE-313

Course Title: Computer Architecture.
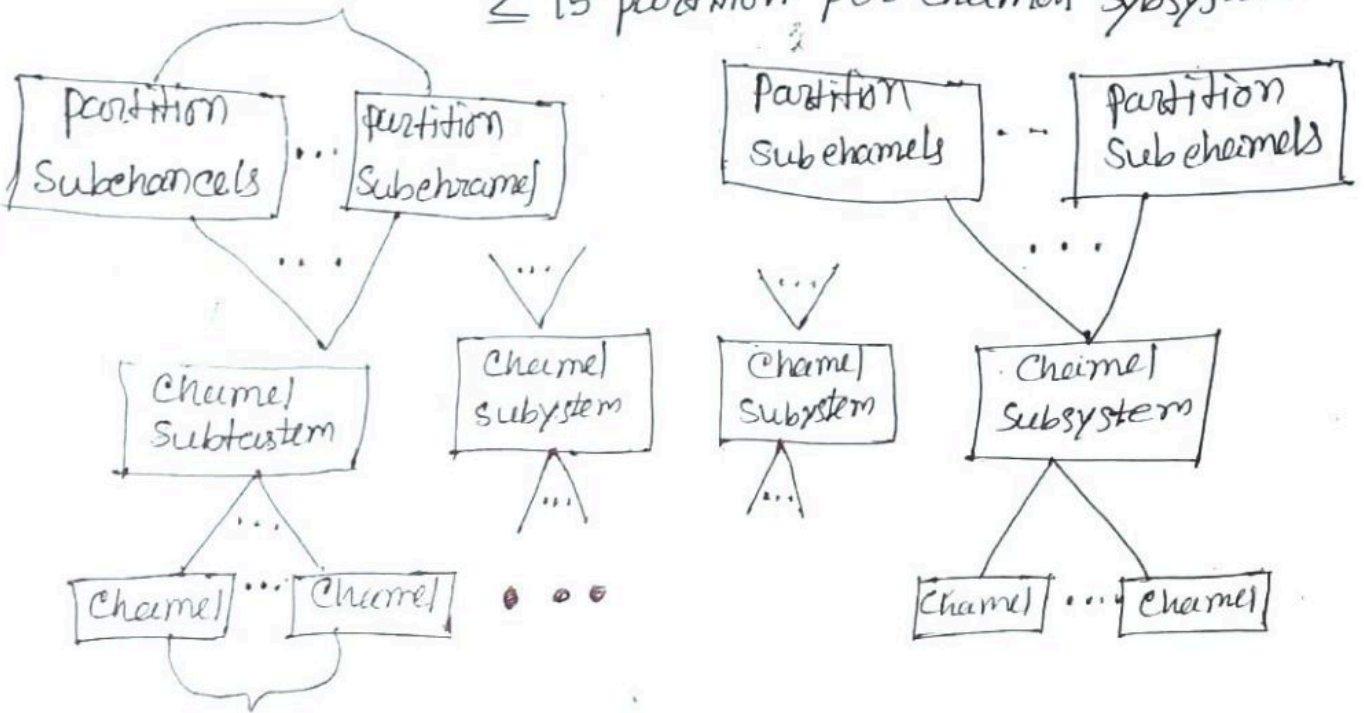
Ans to the ques No. 1 (a)

The 2EC12 I/O subsystem is similar to the one on 2196 and includes a pcie infrostructure. The I/O Subsystem is supported by both a pcie bus and on I/O bus similar to that of 2196. It includes the in-finiband double date reate (IB-DDR) infrastructure which replaces the self-timed intrastructure is designed to reduce processor usage, the latencys and provide increased throughput. The I/O enpansion network uses the infinband link layer (IB-2, Double Data Rate).

EC12 also affers three I/O infrastructure elements for holding the I/o features: PCI e I/O drawers, for PCIe features; and I/O drawers and I/O cages, for non-pcIe features.

3.

Channel Structure:

$\leq$ 15 partition per channel subsystem

$\leq$ 256 channels per channel Subsystem

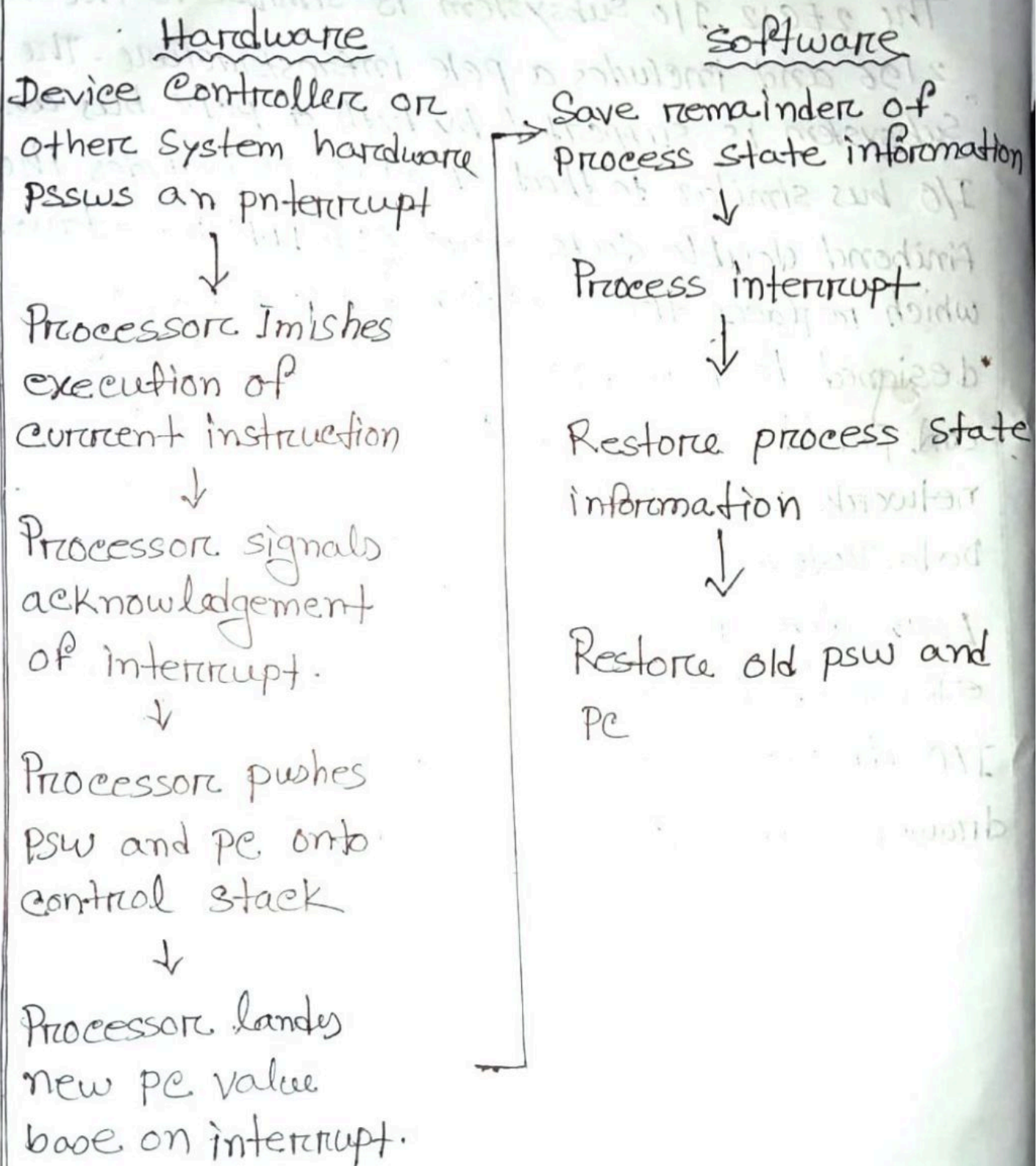$\leq$ 1024 partition per subsystem

Fig:- IBM ZEC12 I/o structure.

Ans to the Q no - 1 (b)

※ When an I/O device completes an I/O operation, the following sequence of hardware events occurs.

① The device issues an interrupt signal to the processor.

② The processor finishes the execution of the current instruction before responding to the interrupt.

③ The processor test for an interrupt and sends an acknowledgement signal to the device that issue the interrupt.

④ The processor now needs to save information needed to resume the current program at the point of an interrupts. The minimum information saved to be is the status of the processor and location of the next instruction to be executed.

⑤ The processor now loads the program counter with the entry location of interrupt handling program.

⑥ The interrupt handler next processes the interrupt.

⑦ After interrupt processing saved register values are —

5.

retrieved from stock and restored and next instruction will be executed:

Hardware	Software
Device Controller or other System hardware Pssws an pnterrupt	Save remainder of Process state information
↓	↓
Processor Imishes execution of current instruction	Process interrupt
↓	↓
Processor signals acknowledgement of interrupt.	Restore process state information
↓	↓
Processor pushes psw and pc onto control stack	Restore old psw and Pc
↓	
Processor landes new pc value base on interrupt.	

Ans to the Q no-1 (c)

⊞ Three techniques for input of a block diagram:-

Programmed I/O: In this method, the CPU stays in a program loop until the I/O unit indietes that is ready for data transfer. It is a time consuring process for the CPU. The programmed I/O method is particularly useful in small low speed computers. The CPU sends the read command to the I/O device and waits in the program loop until it receives a response from the I/O device.
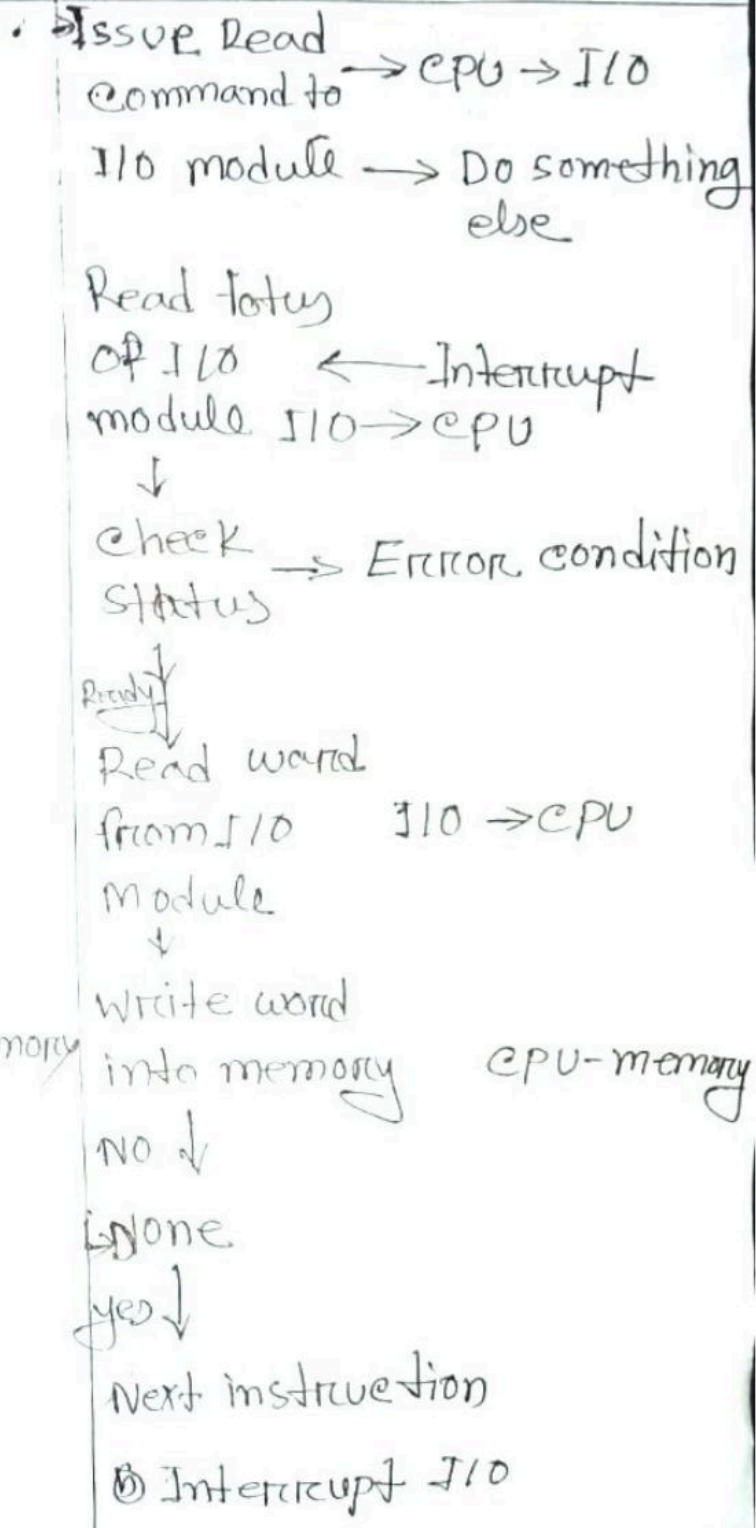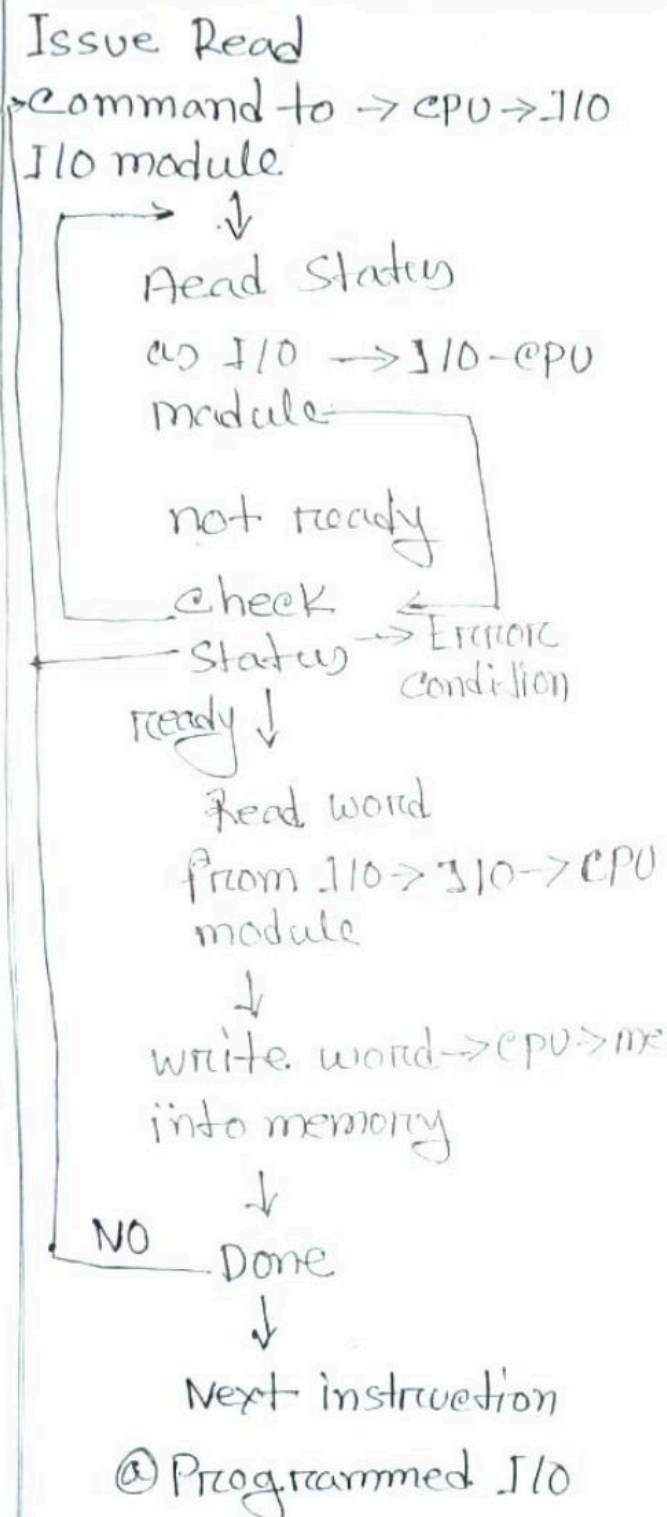
Interrupt I/O: The problem with programmed I/O is that the CPU has to wait for the ready signal from the I/O device. So alternative to this is interrupt I/O. In this method, the CPU issues a read command to the I/O device about the status. When the I/O device is ready it sends an interrupt signal to the processor. When CPU recieves the signal from the device, it checks the status. If the status is ready, then the CPU read the word from the I/O device and writes the word in the main memory.

If its done success—Fully, than the processor will go to the next Instruction.

Direct Access Memory (DMA): Leting the DMA controller (DMAC) is to manage the memory buses directly. It would ~~Pm~~ improve the Speed of data transfer. A chip. says a DMA controller (DMAC) Manages this process. The CPU is idle and it has no control over the memory buses. A DMA controller takes over the buses to manage the transfer directly between the I/O device, and memory

(8)

Issue Read
command to → CPU → I/O
I/O module.
    → ↓
    Read Status
    as I/O → I/O-CPU
    module

    not ready
    check ←
    Status → Error
            condition
ready ↓
    Read word
    from I/O → I/O → CPU
    module
    ↓
write word → CPU → memory
into memory
    ↓
NO   Done
    ↓
    Next instruction
    ⓐ Programmed I/O

Issue Read
command to → CPU → I/O
I/O module → Do something
               else

Read Status
of I/O   ← Interrupt
module I/O → CPU
    ↓
check → Error condition
Status
Ready ↓
Read word
from I/O   I/O → CPU
Module
    ↓
Write word
into memory   CPU - memory
NO ↓
↳ Done
yes ↓
Next instruction
ⓑ Interrupt I/O

Issues Read   CPU $\rightarrow$ DMA

black command $\longrightarrow$ Do something

to I/O module   else

Read status

of DMA $\longleftarrow$ Interrupt

module $\longrightarrow$ CPU

$\downarrow$

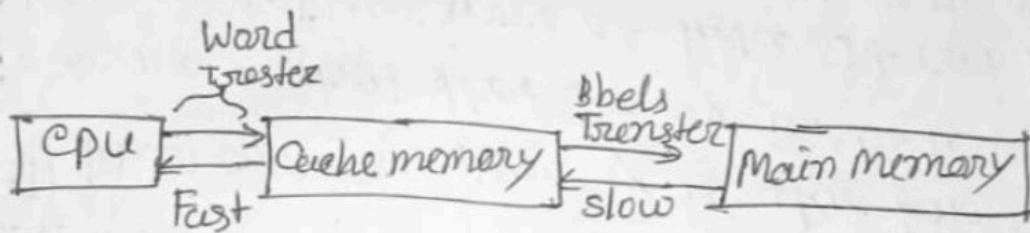Next instruction

(c) Direct Memory access.

Ans to the Ques No—2(a)

☐ Cache Memory:-

Caches memory is a small and high speed access area. It is used to store frequently accessed data. Wherever it is required. this data is made avaible to the central processing unit at a rapid rate. This memory often resides in the cpu. It has been devised to match the speed of the processar. it is statia - RAM. SRAM. These are faster. Cache memory is located between main memory and cup. It a processar needs to write or read a location in the main memory. it checks the availability of the memory location in the memory location the cache. It's done by comparing the address of the memory location to all legs in the cache with have the possibility of containing that particular address.

☐ Main memory:- Memory is also know as RAM. It is memory unit that directly intereats with the CPU. It is a volatile source of data. It can be described as a large array comprising of words or bytes. RAM is connected with the processar by its address and data buses. This buses are compresed as electrical circuits or bits. Main memory is atually built from DRAM chips or Dynic RAM. They are known for their compact size and capsbility for a faster acess. It is important to mention that the Computer an only manipublate

data that is present in the main memory. A typical module of desktop memory is long and thin in appearance. It is installed in the memory module slots present on the motherboard. Modern memory modules come in various capacities. like 256 mb, 512 mb, 1gb, 2gb, 4gb, 8gb sizes, main memory has a limited capacity.

Word
Transfer
| CPU | → | Cache memory | → | Main memory |

Fast
Bbels
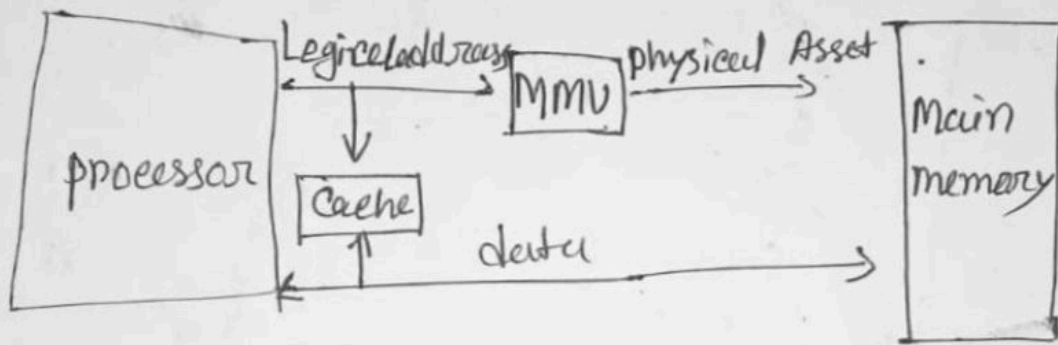Transfer
slow

Ans to the ques No – 2(b)

Logical cache:- with a logical cache the tag information refers to the logical addresses currently in use by the executing task. It the task is switched out during context switch, the cache tags are no longer valid and the cache, together with its often hard-won data must be flushed and cleared. The processor must now go to much main memory to tech the first before any benefit is obtained from the cache. However, cache accesses do not need to go through the MMU and do no suffer from any associated delay.

physical cache:- physical cache use physical addresses. do not need flushing on a context switch and therefore data is preserved within the cache. The disadvantage is that all accesses must go through the memory management unit, thus incurring delays. Particular
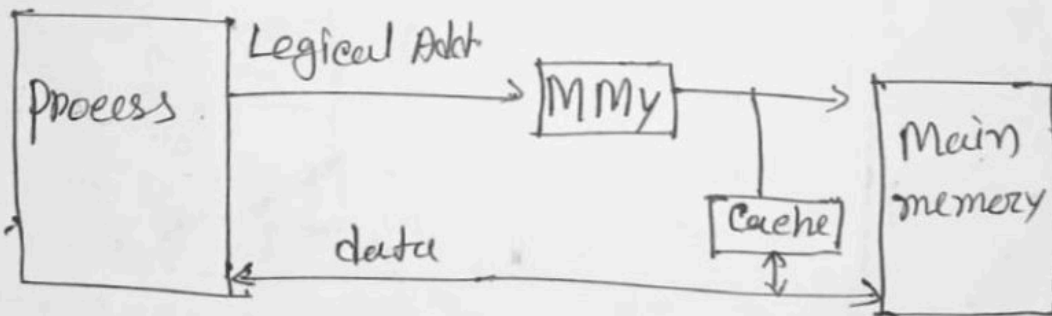
Care must also be exercised when pages are swapped to and from disk.

It the processor does not invalidate any associated cache entries, the cache contents will be different from the main memory contents by virtue of the new page that has been swapped in.
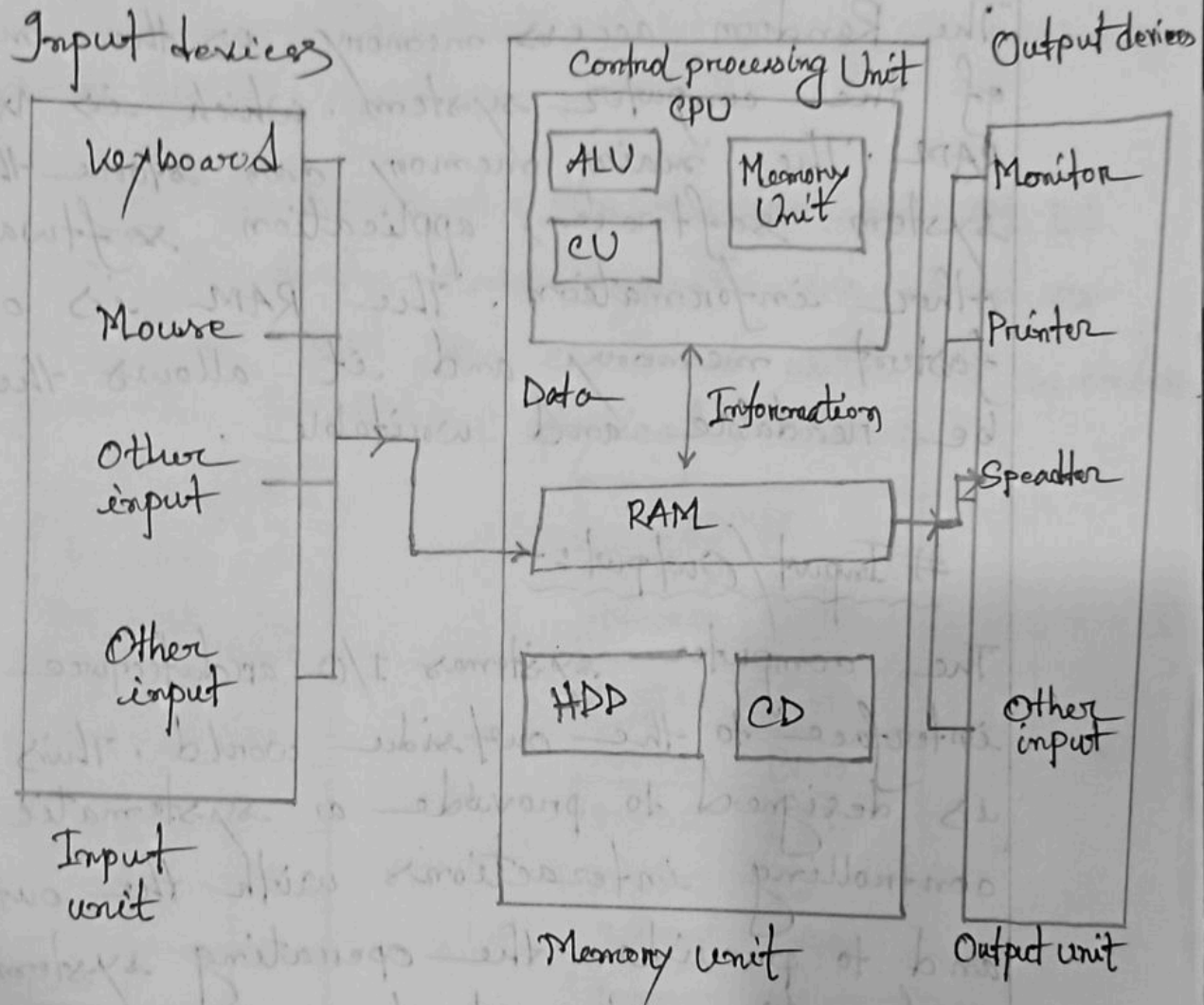

a) Logical caches

b) Physical cache.

Answer to the question no: 3 (a)

Ans: Computer System:—

Input devices

Output devices

Control processing Unit
CPU

| ALU | Memory Unit |
| CU | |

Data   Information

RAM

HDD   CD

Input unit

Memory unit

Monitor

Printer

Speaker

Other input

Output unit

Keyboard

Mouse

Other input

Other input

Control processing unit:—

Control Unit:— ALU, CU, Memory unit

Memory Unit:— RAM, HDD, CD.

P.t.o.

Main components and interactions with the main memory and I/O:—

Main Memory:

The Random access memory is the main memory of the computer system. which is known as RAM. The main memory can store the operating system software, application software and other information. The RAM is one of the fastest memory and it allows the data to be readable and writable.

Input/Output:—

The computer systems I/O architecture is its interface to the outside world. This architecture is designed to provide a systematic means of controlling interactions with the outside world and to provide the operating system with the information it needs to mange I/O activity effectively.

Answer to the question no: 3 (b)

Ans: Indirect addressing for x86 :—

In register indirect addressing mode, the address of the memory location where the operand resides is held by a register.

The register used for the purpose are SI, DI and BX. If these three register are used as pointer they must be combined with DS in order to generate the 20 bit physical Address.

Processor register		
AX	AH	AL
BX	BH	BL
CX	CH	CL
DX	DH	DL
SI		
DI		
BP		
SD		
CS		
DS		
SS		
ES		

Memory	
Memory Address	Data
10000	AAH
10001	BBH
10002	CCH
10003	EEH
10004	DDH
10005	EEH
10006	FFH
10007	11H
10008	22H
10009	03H
10094	44H