Victoria University of Bangladesh
Department of CSE
Program:- B.Sc in CSIT
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Course title:- Microprocessor and Interfacing
Course code:- CSE 413

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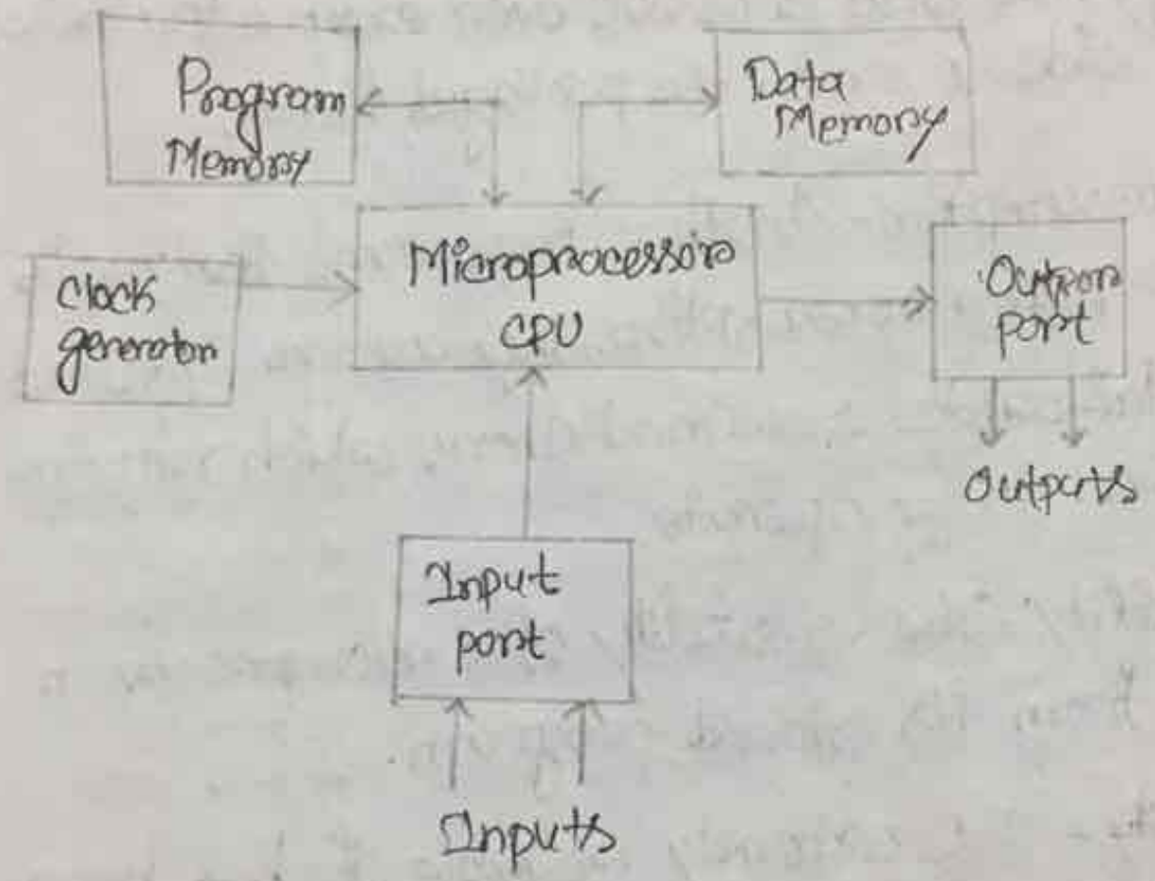
Batch:- 20

Mid Assesment

(1)

Ans to the Q no 1(a)

(i) Block diagram of a basic Microcomputer:-



(ii) Features of Microprocess:-

(i) Low cost:- The most important characteristics of a microprocessor is its low-cost availability. Because of the widespread use of microprocessors,

the volume of production is very high.

(iv) Size:- The second key feature of the microprocessor is its small size. As the improvement in fabrication technology, its size does not even exceed a few inches on any side, even in the packaged form.

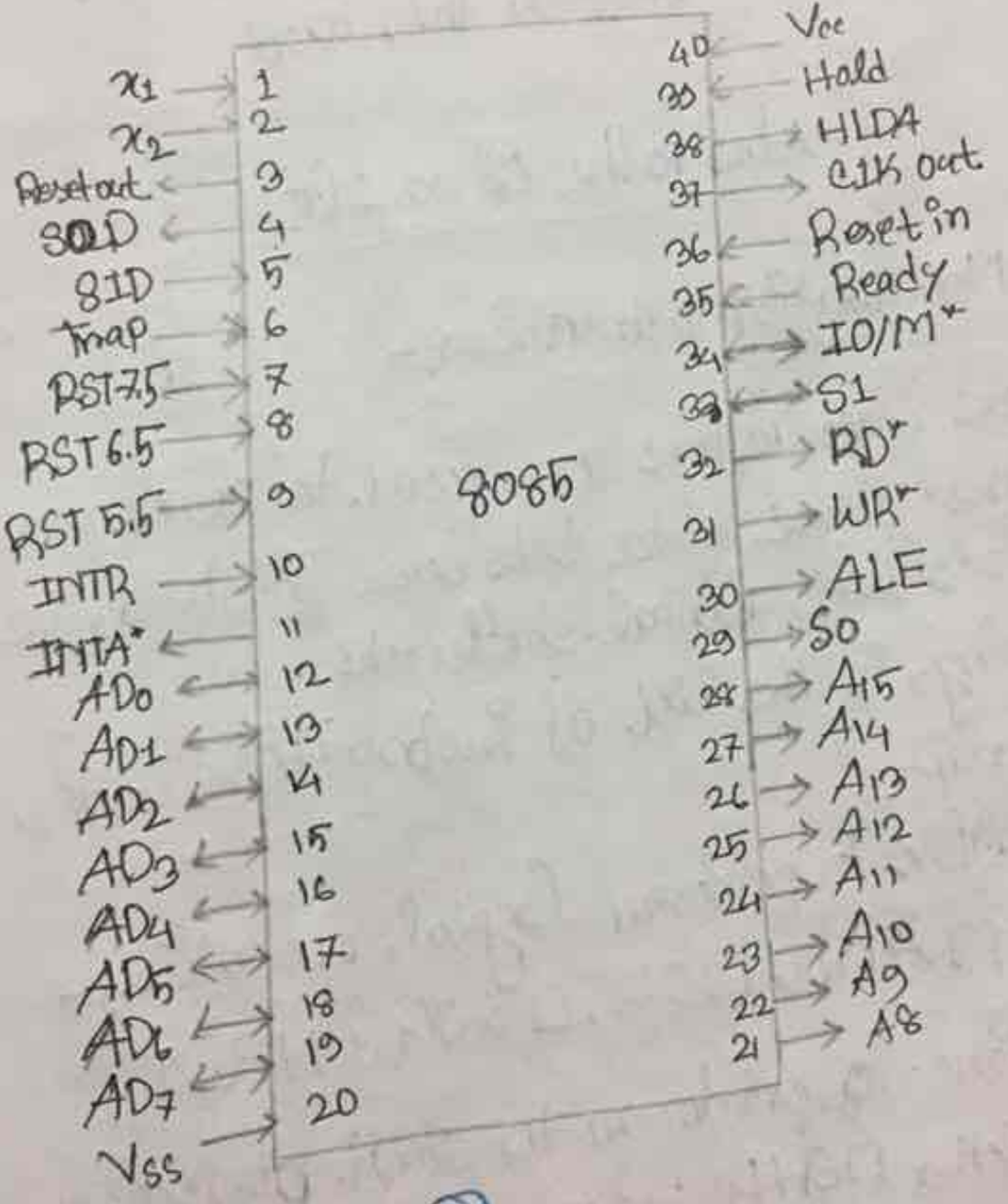
(v) Power consumption:- Another important feature is its low power consumption. They are manufactured by Metal-oxide semiconductors which require low power to be operate.

(vi) Versatility:- The versatility of a microprocessor results from its stored program.

(vii) Reliability:- Its extenely reliable. It has been found that the failure rate of an IC is relatively low at the packaging level.

Ans to the Q no 2(a)

(a) Architecture of 8085:-



Intel 8085 is fabricated as a 40-pin DIP IC. DIP ~~stat~~ stands for 'dual inline package'. It means the package will have pins on only 2 sides, 20 on each side in this case.

Ans to the Q no 1(c)

(i) Bit Manipulation Instructions:-

These instructions are used to perform operations where data bits are involved, i.e. operations like logical, shift, etc.

Following is the list of instructions under this group

Instructions to perform logical operations -
□ NOT, □ AND, □ OR, □ XOR, □ TEST

Instructions to perform to shift operations-
□ SHL/SAL, □ SHR, □ SAR

Instructions to perform rotate operations:-
□ ROL, □ ROR, □ RCR, □ RCL.

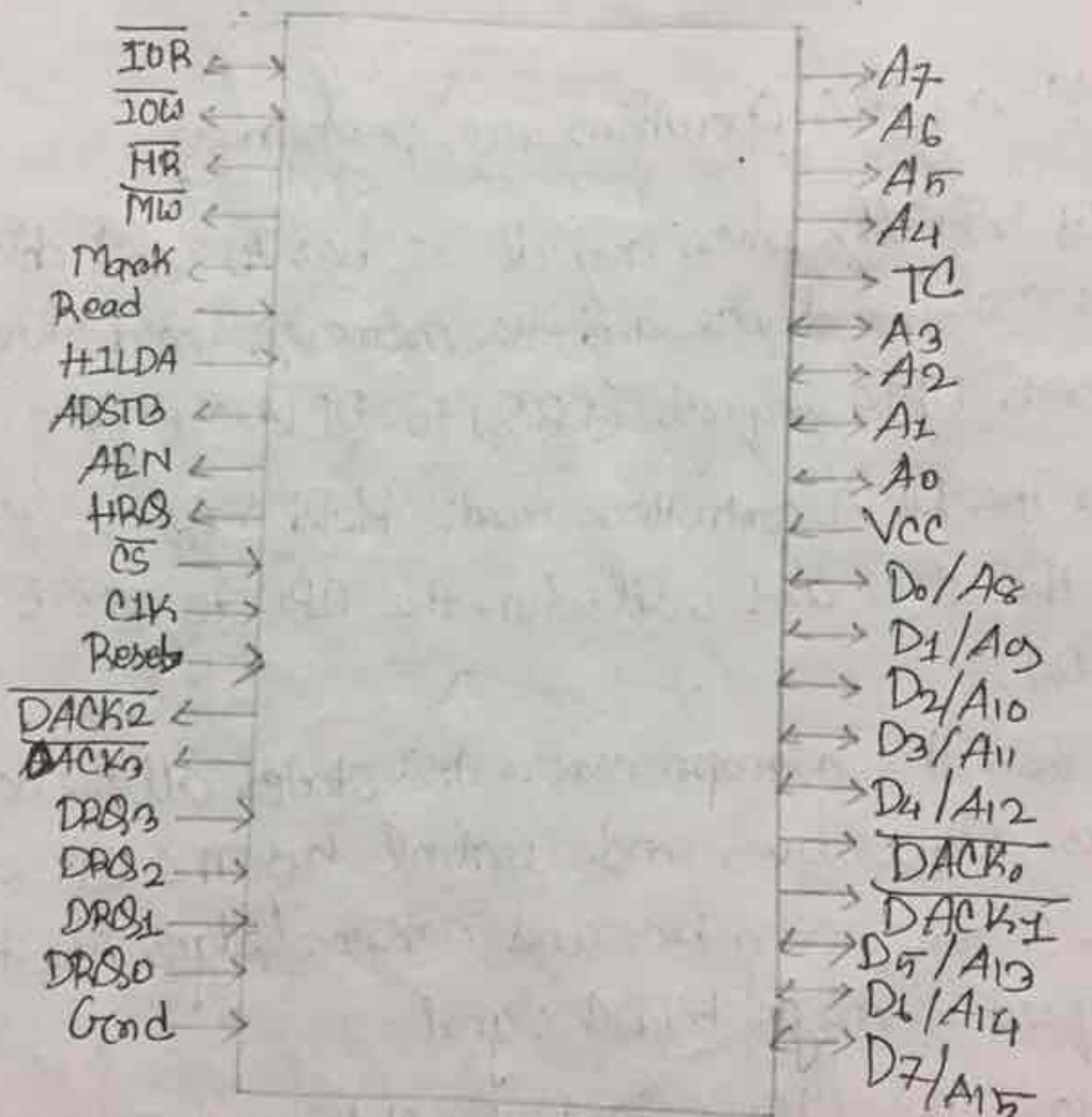
Ans to the Q no-2(a)

① How DMA Operations are performed:-

- Initially, when any device has to send data between the device and the memory, the device has to send DMA request (DRQ) to DMA controller.
- The DMA controller sends Hold request (HRQ) to the CPU and waits for the CPU to assert the HLDA.
- Then the microprocessor tri-states all the data bus, address bus, and control bus. The CPU leaves the control over bus and acknowledges the HOLD request through HLDA signal.
- Now the CPU is in HOLD state and the DMA controller has to manage the operations over buses between the CPU, memory and I/O devices.

Ans to the Q no-2(b)

④ Descriptions of the pins of 8257:-



Intel 8257

40-pin DIP

DRQ_0 to DRQ_3 - Pin(16-19) - This pins get enabled whenever the input device requests the DMA controller for direct data transfer the main memory.

$DACK_0$ to $DACK_3$ - Pin(14, 15, 24, 25) - This are active low signals that are nothing but acknowledgement signal generated by the controller to show the acceptance of DMQ by the peripheral devices.

IOR - Pin 1 - In the master mode of operations, the low signal at this pin indicates the read operation, while in slave mode, it shows that read operation is performed over the internal register by the processor

IOW - Pin 2 - It indicates write operation in masters mode. In slave mode the data bus loads its content at the register.

$D_0 - D_7$ - Pin (26-30 & 21-23) - These are data lines that hold commands and status words in slave mode. While in the master mode it transfers higher address bytes to the latch.

A_0-A_3 - Pin(32-35) - This are 4 least significant address lines that act as input and output in slave and masters operating mode of the system respectively.

A_4 to A_7 - Pin(37-40) - These are basically lower order address lines, produced by the controller in master mode.

CLK - Pin 12 - This pin is used to provide an internal clock frequency signal to 8257.

CS - Pin 11 - CS denotes chip select and it is an active low pin.

HRQ - Pin 10 - The enabling of this pin shows the request to directly access the memory by the peripheral device for read-write operation.

HLDA - Pin 7 - The enabling of this pin represents the acknowledgement by the processor in response to HOLD signal of the DMA controller.

MEMR - Pin 3 - A low signal at this particular pin represents that read operations is performing over the memory by the peripheral device.

MEMW - Pin 4 - A low active pin that gets enabled at the time of memory write operation by the peripheral device.

ADSTB - Pin 8 - It stands for address strobe. Enabling this pin will demultiplex the address and data bus using latches.

Vcc - Pin 31 - The signal for the operation is applied at this pin.