Victoria University
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Dept. of CSE
Program:- BSc in CSIT
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Course title:- Computer Architecture
Course code:- CSE 313

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Batch:- 20

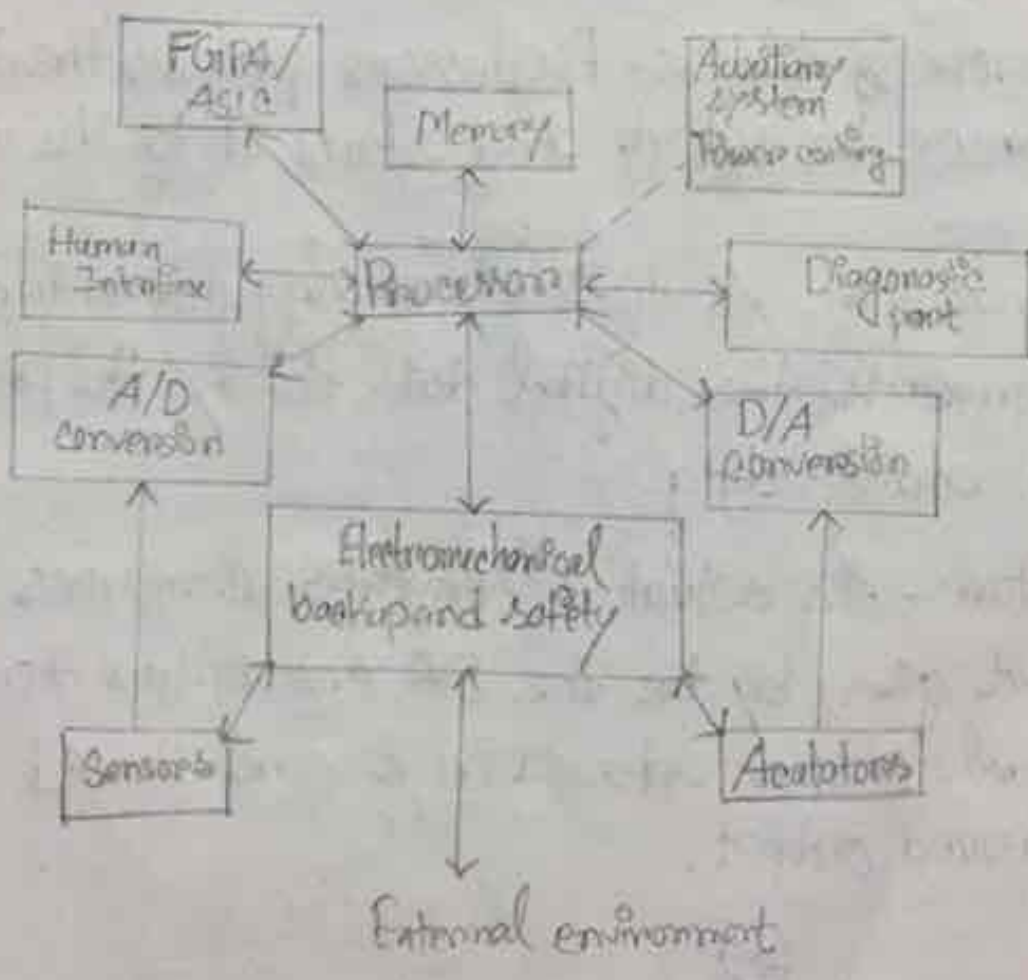
Mid Assesment

1

Ans to the Q. no (1)-(a)

Here is a diagram of,

Possible Organization of an Embedded System:-



☐ Sensors:- It measures the physical quantity and converts it to an electrical signal which can be read by an observer, or by an A2D converter.

☐ A-D converter:- An analog-to-digital converter converts the analog signal sent by the sensor into a digital signal.

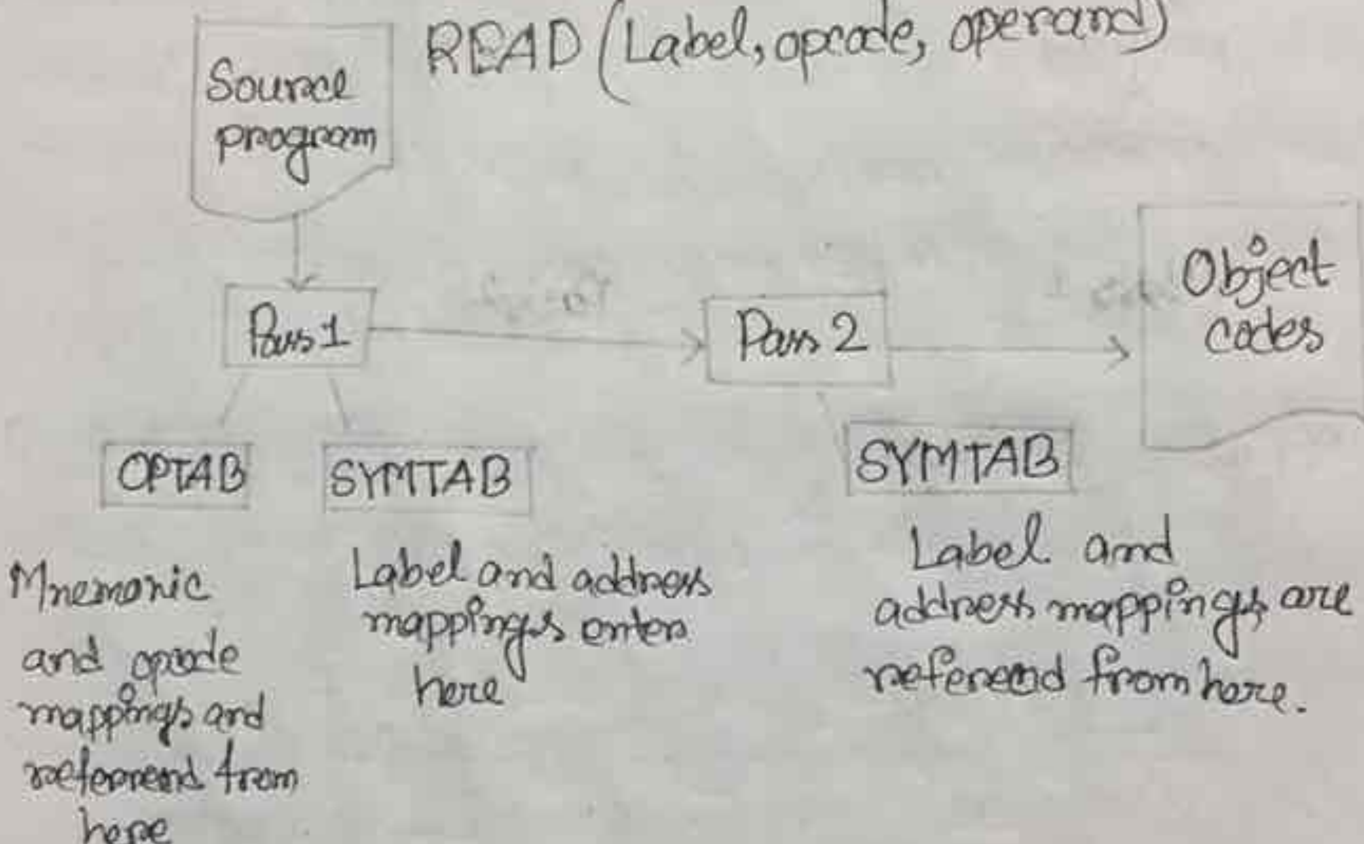
☐ Processor & ASICs:- Processors process the data to measure the output and store it to the memory.

☐ D-A converter:- A digital to analog converter which converts the digital data fed by the processor to analog data.

☐ Actuator:- An actuator ~~converts~~ compares the output given by ~~the~~ the DA converter to the actual output stored in it and stored the approved output.

Ans to the Q no-(1)-(b)

A simple two pass assembler Implementation:-



A two-pass assembler solves this dilemma by devoting one pass to exclusively resolve all (data/label) forward references and the general object code with no hassles in the next pass. If a data symbol depends on another and this another and this another depends on yet another, the assembler resolved this recursively.

Ans to the Q no - (1) - (c)

☐ Three-level cache organization:-

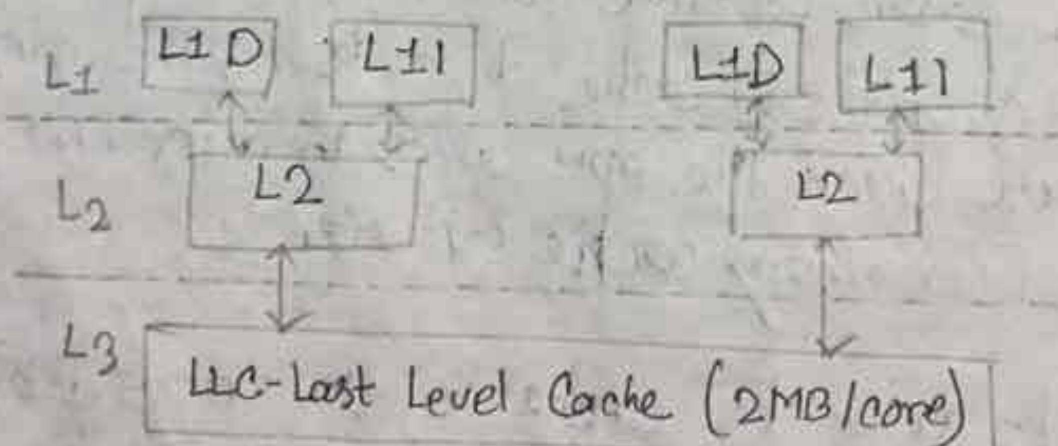
(1) L_1 cache - is the fastest memory that is present in a computer system. CPU is most likely to need the L_1 cache at first while completing a task. The size of the L_1 cache depends on the cpu, so you must check the cpu specs to determine the exact L_1 memory cache ~~ser~~ size.

(2) L_2 cache:- L_2 cache is slower and bigger in size than L_1 cache. Where L_1 cache measures in kilobytes, modern L_2 cahes measures in mega-

bytes. When it comes to ~~ep~~ speed ~~to~~ the L_2 caches lags behind the L_1 cache but still much faster than RAM.

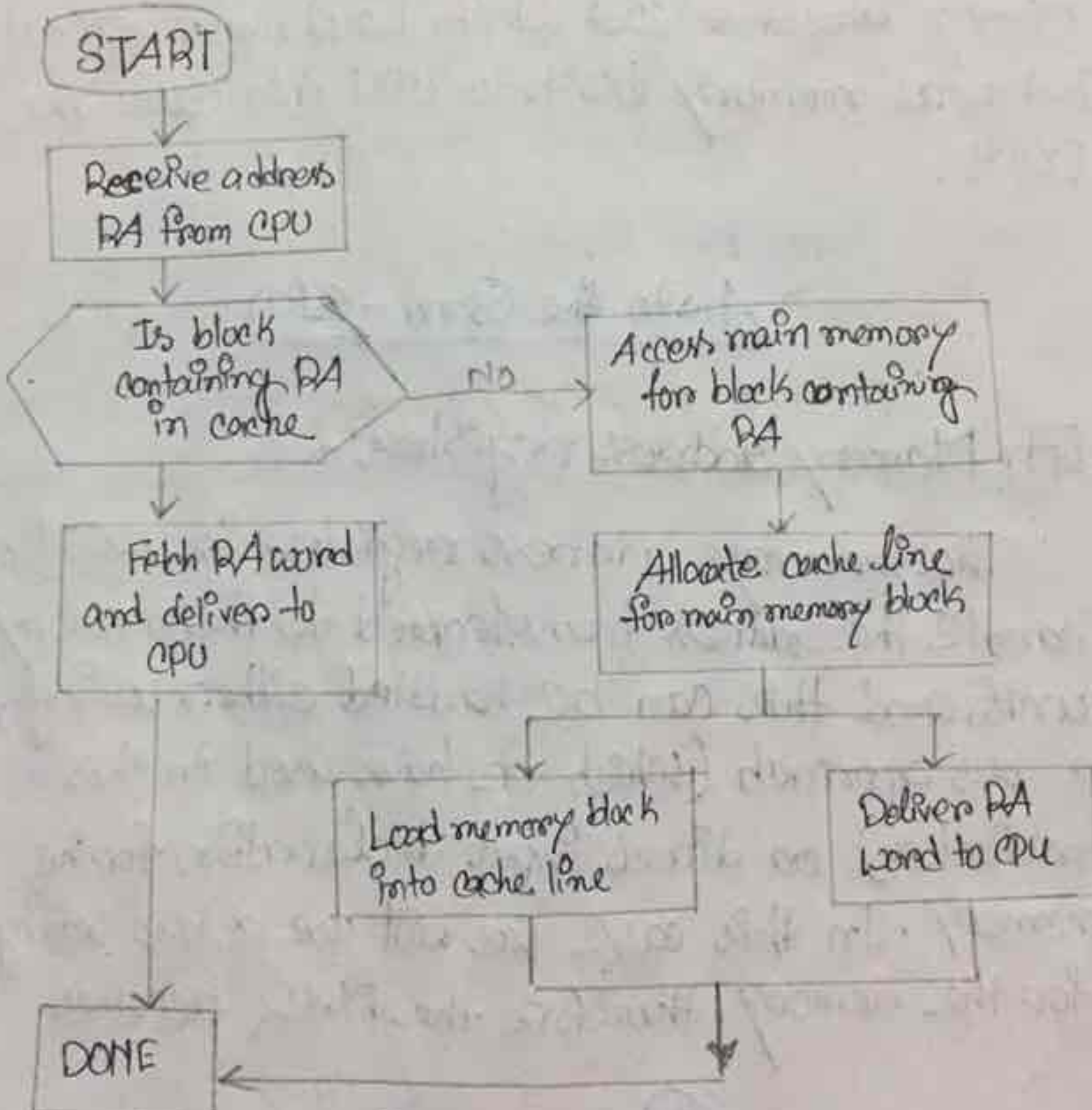
③ L_3 cache:- In the early days the L_3 memory cache was actually found on the mother-board. This was a very long time ago, back when most cpu-s were a single core processor. Now the L_3 cache can be massive, with top-end consumer CPUs featuring L_3 caches up to 32mb.

The L_3 cache is the largest and slowest. Modern CPUs include the L3 cache on the cpu itself.



Ans to the Q no- 2(b)

Cache Read Operation:-



-START Recieve address RA from CPU is block containing RA no access main memory for block containing RA in cache? Yes Fetch RA word Allocate cache and deliver line for main to CPU memory ~~block to CPU~~ block Load main Deliver RA word memory block to CPU into cache line DONE.

Ans to the Q no - 2(a)

☐ Memory address register:-

The memory address register is used to handle the address transferred to the memory unit, and this can be handled either using a bus approach (which we have used in this architecture) or direct input declaration for the memory. In this case we will use a bus setting for the memory, therefore the MAR becomes a simple register which sets its output to the value of the required address from the IR or PC when its control signal mar-load is high. The Memory Address Register (MAR) in a simple microprocessor needs enough bits for the address. For example, if the address requires 8 bits then the size of the register needs to be 8 bits wide. The 'MAR' therefore has clock and reset signals, and also the same interface to the internal processor bus (mar-bus) defined as a standard logic of direction inout, however only the first 8 bits are used.

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