Name : Abdullah Bin Noman Tabid

Student ID : 2120190031

Course Code : CSE-413

Course Title : Microprocessor

* Mid-term

(Exam)

Ans to the Q No 1(a)

Block Diagram:

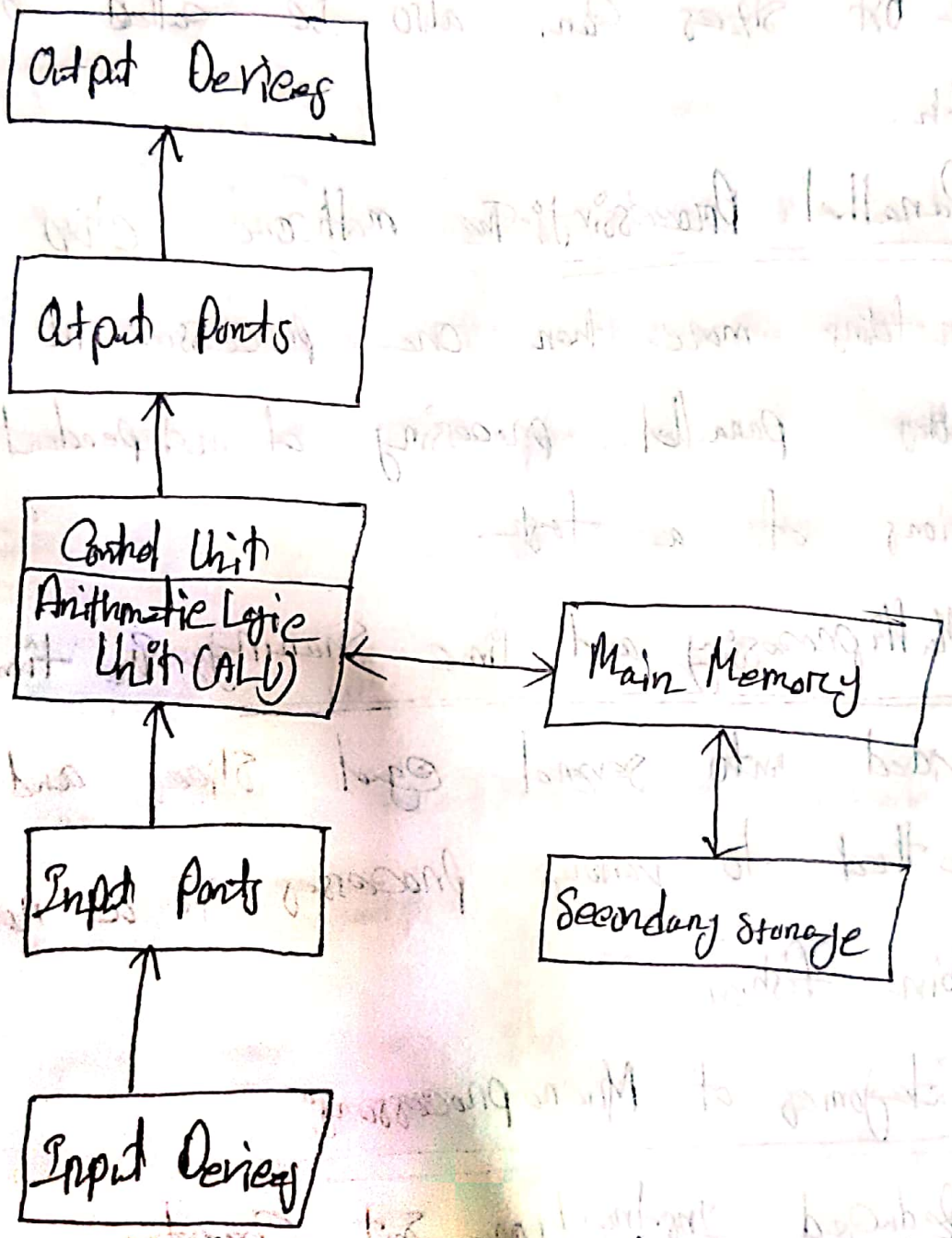

Fig- Block diagram of a Computer

Features of microprocessor:

① **Architecture:** Microprocessors are available in 8 bit, 16 bit, 32 bit, 64 bit architectures. The bit sizes can also be called bus width.

② **Parallel Processing:** The multicore chip that contains more than one processor in it, enables parallel processing of independent portions of a task.

③ **Multiprocessing and Time Sharing:** The time is divided into several equal slices and it is allotted to various processes in a round-robin fashion.

④ **Categories of Microprocessors:**

(a) Reduced Instruction Set Computer.

b) Complex Instruction Set Computer.

d) Special Purpose Processors.

Ans to the Q No 1 (c)

Bit manipulation instructions sets (BMI sets) are ~~extentions~~ extensions to the x86 instruction set architecture for microprocessors from Intel and AMD. The purpose of these instruction sets is to improve the speed of bit manipulation. All the instructions in these sets are non-SIMD and operate only on general-purpose registers.

There are two sets published by Intel: BMI and BMI2; they were both

introduced with the Bulldozer micro-architecture with BMI1 matching features offered by AMD's ABM instruction set and BMI2 extending them. Another two sets were published by AMD: ABM and TBM (Advanced Bit Manipulation, which is also a subset of SSE 4a implemented by Intel as part of SSE 4.2 and BMI1), and TBM (Trailing Bit Manipulation), and extension introduced with Piledriver based processors as an extension to BMI1, but dropped again in Zen-based processors).

Ans to the Q No 1 (c)

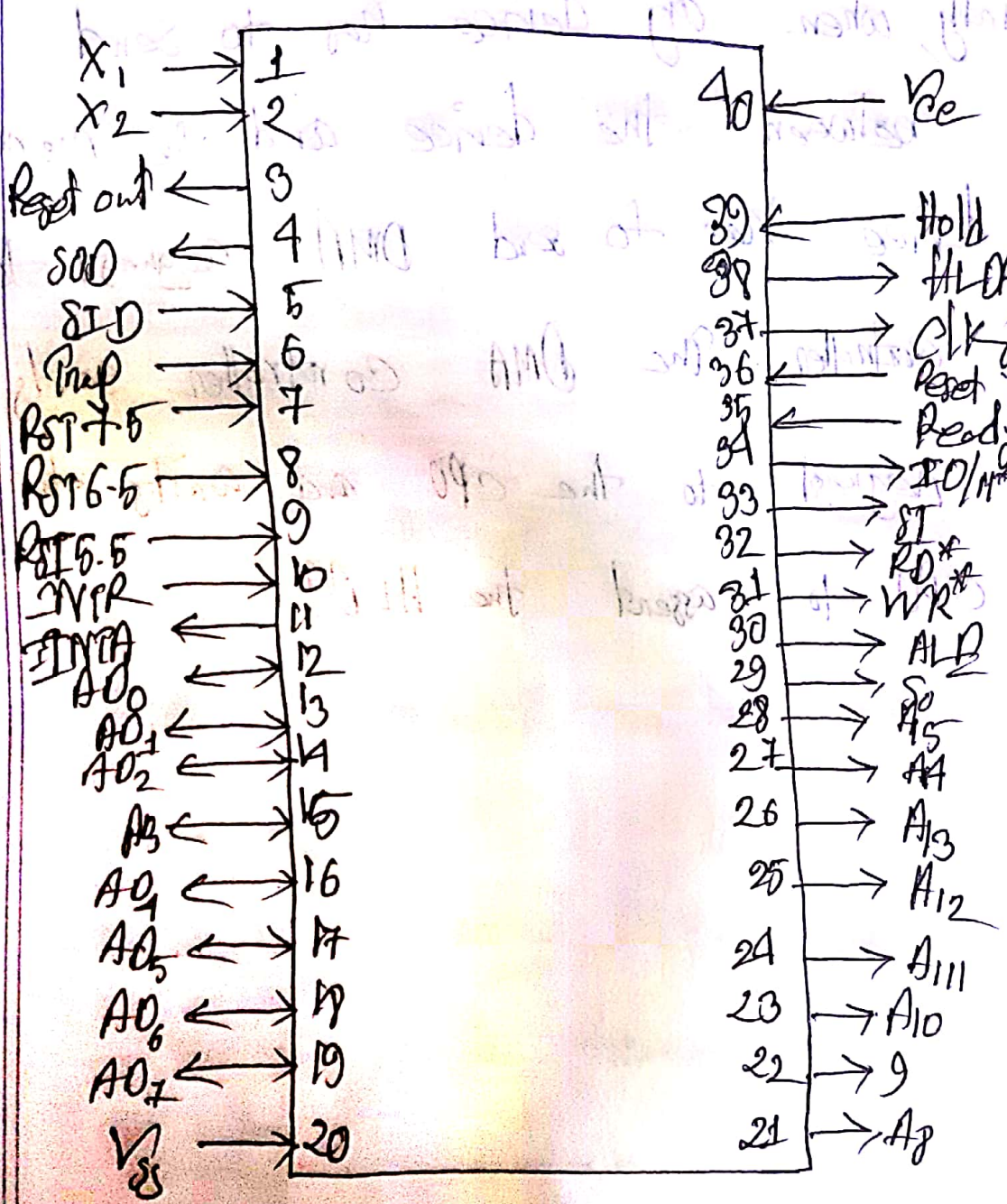

Fig: Pin diagram of 8086

Ans to the Q. No 2(a)

Initially, when any device has to send data between the device and the memory, the device has to send DMA request to DMA Controller. The DMA Controller sends Hold request to the CPU and waits for the CPU to assert the HLDA.

Ans to the Q No 2 (b)

Features of 8257:

a) It has four channels which can be used over four I/O devices.

b) Each channel has 16-bit address and 14-bit counter.

c) Each channel can transfer data up to 64KB.

d) Each channel can be programmed independently.

e) Each channel can perform read transfer, write transfer and verify transfer operations.

f) It generates MARK signal to the peripheral device that 128 bytes

have been strengthened.

g) It requires a single phase clock.

h) Its frequency ranges from 250KHz to 3MHz.

i) It operates in 2 modes, Master mode and slave mode.

These are the main features of 8257 pin description.

These things are very important for any 8257 pin description.

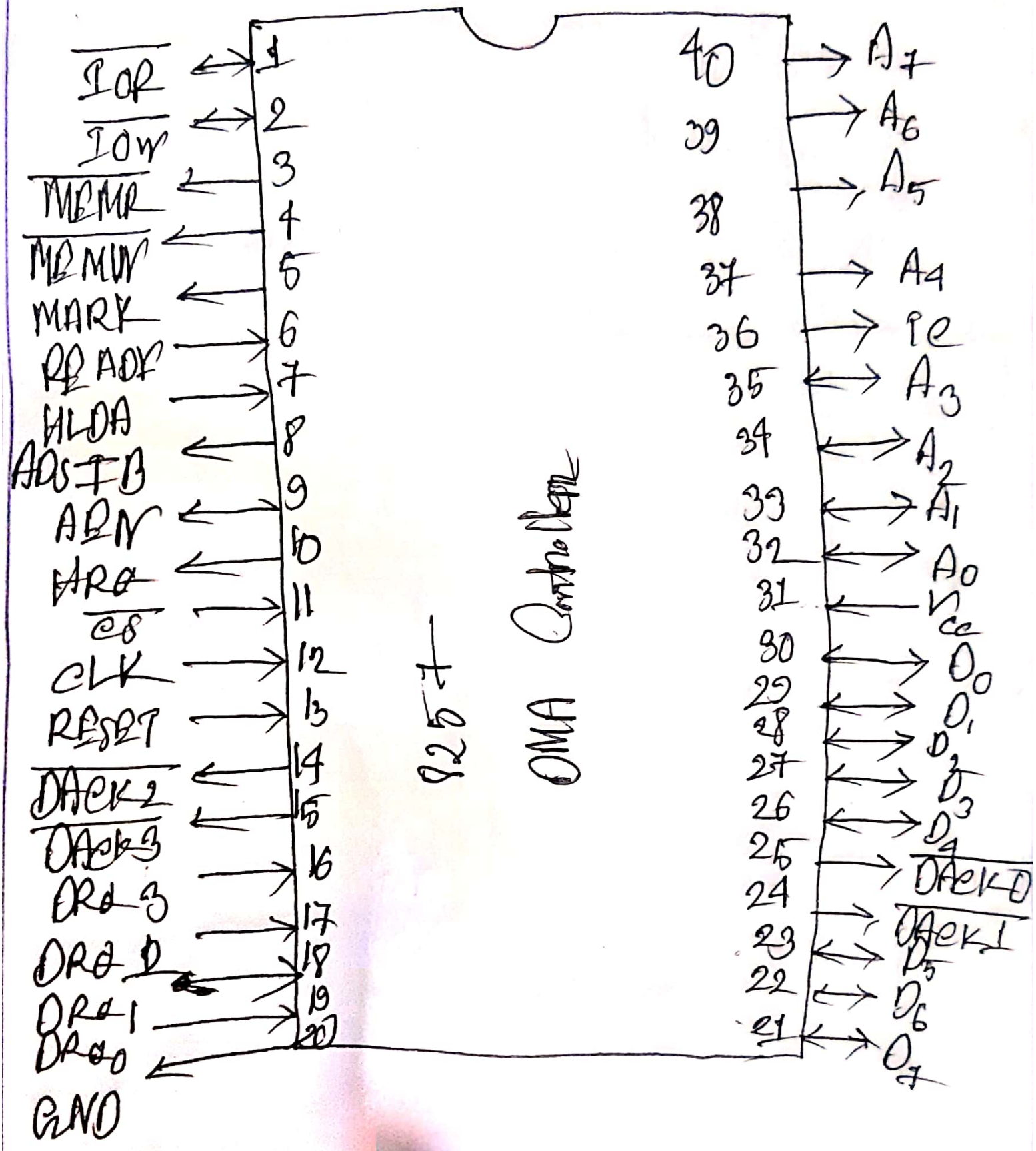

Fig. Pin diagram of 8257.