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Dept: CSE (E)

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Course code: CSE 313

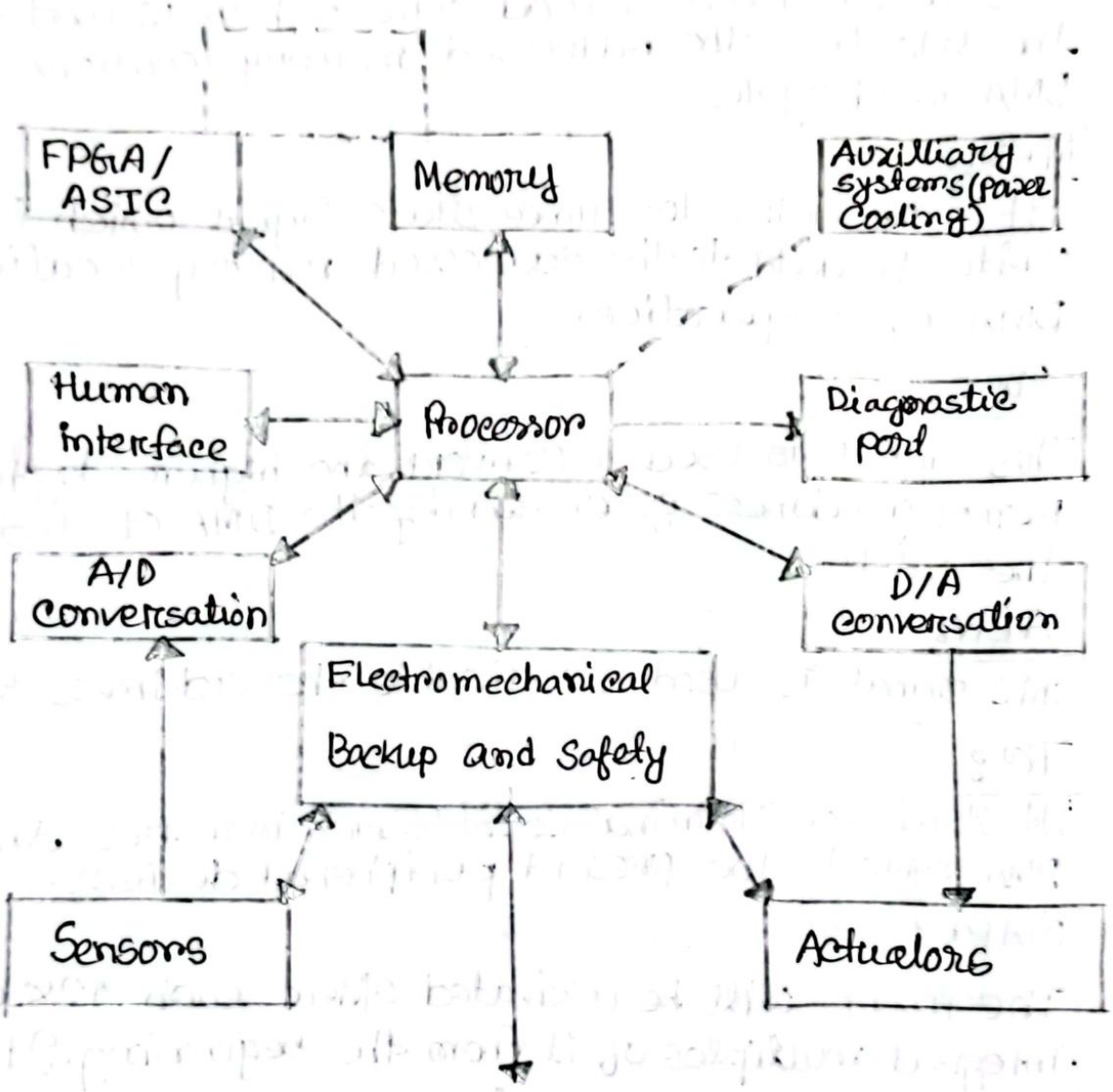
Course Title: Computer Architecture

01

Fall-2022
Mid Assessment
CSE-313

Ans to the Qus NO : 01 (a)

Ans: Possible organization of an Embedded System:



Possible organization of an Embedded system.

02

An Embedded system is a Microprocessor-based computere hardware system with software that is designed to perform a dedicated function, either as an independent system or as a part of a large system. At the core is an inte-grated circuit designed to carrey out computation for real-time operations.

The basic structure of an embedded system includes the following components:

→ Sensor:

The sensor measures and converts the physical quantity to an electrical signal, which can then be read by an embedded systems engineer or any electric instrument A sensor stores the measured quantity to the memory.

→ A-D Converdere :

An analog-to-digital converdere converts the analog signal sent by the sensor in-to a digital signal.

→ Processor & ASICs:

Processors assess the data to measure the output and store it to the memory.

→ D-A converdere:

A digital-to-analog converdere changes the digital data fed by the processor to analog data.

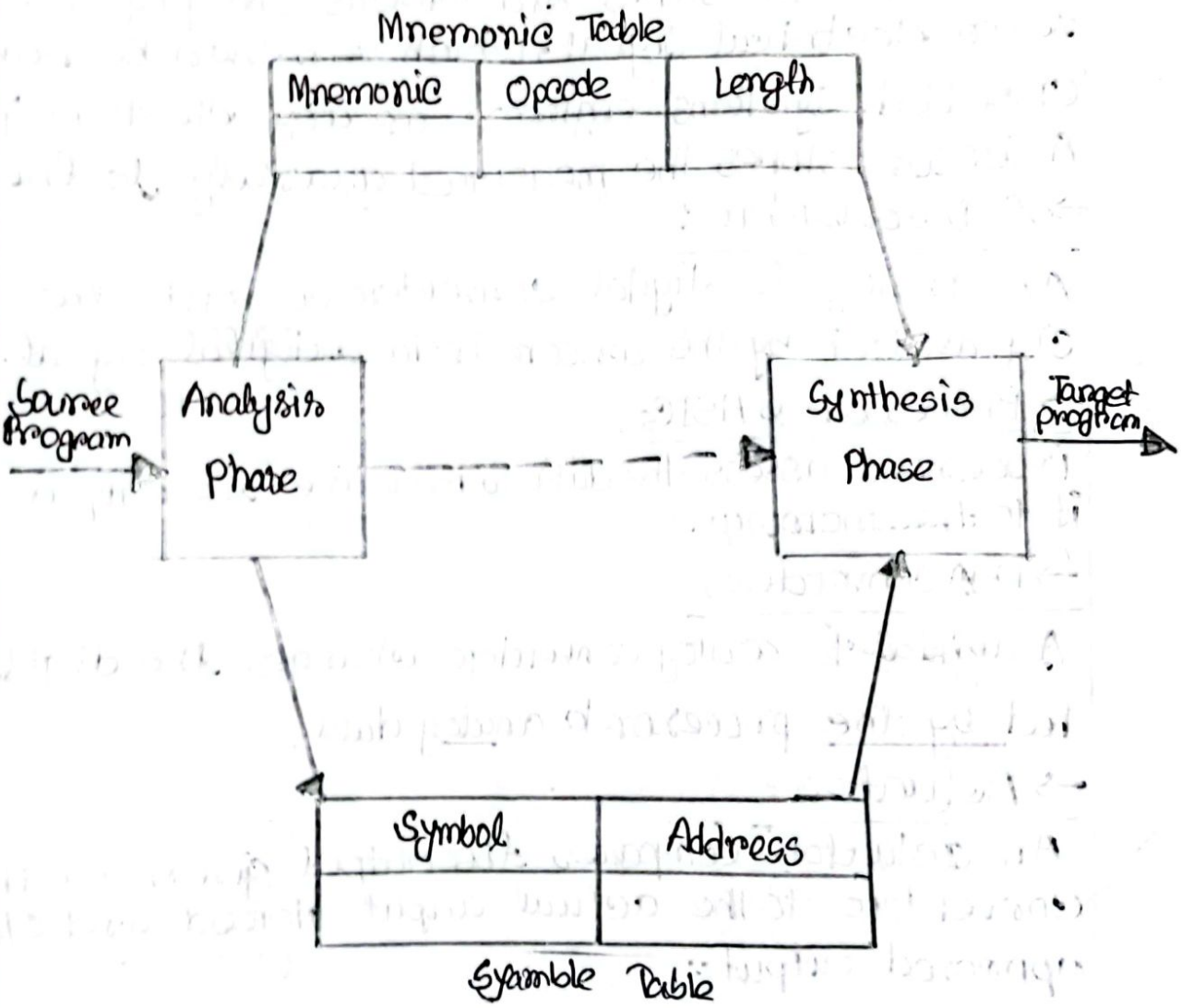
→ Actuator:

An actuator compares the output given by the D-A converdere to the actual output stored and stores the approved output.

Ans to the Que No : 01 (b)

Ans: One-pass assemblers:

A one pass assembler passes over the sourcefile exactly once, In the same pass collecting the labels, resolving future references and doing the actual assembly. The difficult part is to resolve future label references (the problem of forward referencing) and assemble code in one pass

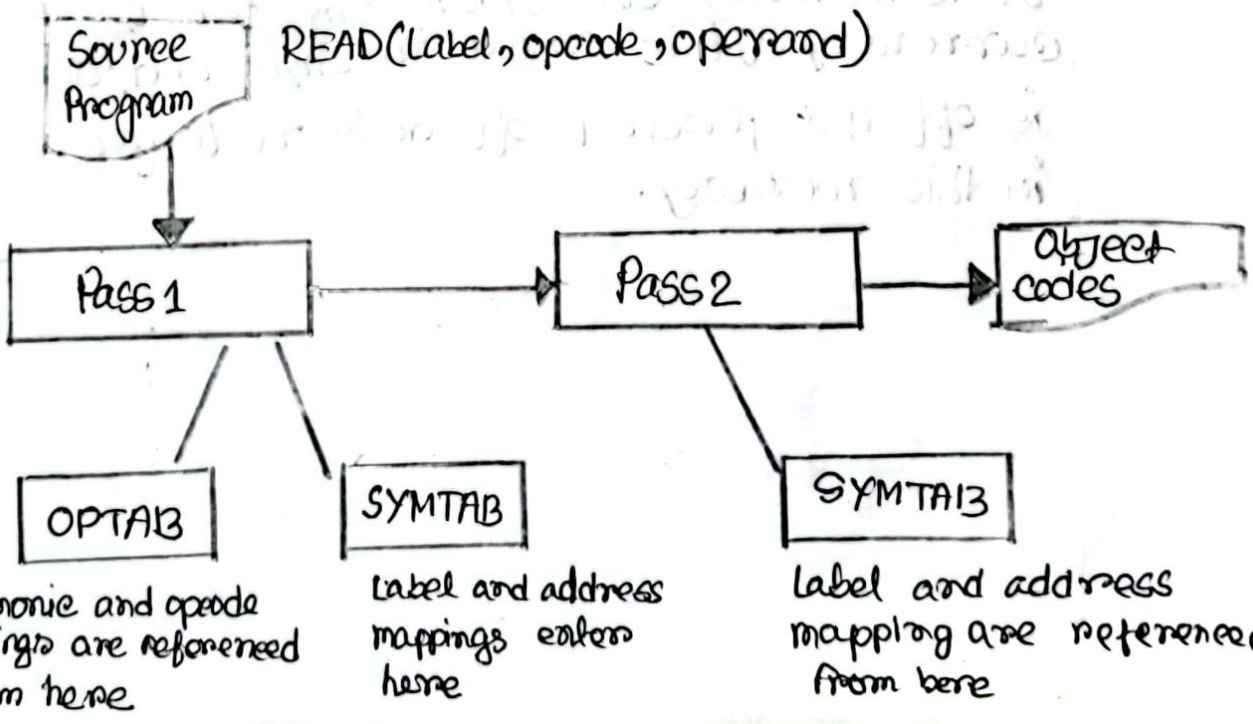


→ Omits the operand address if the symbol has not yet been defined.
→ Enters the undefined symbol into SYMTAB and indicates that it is undefined
→ Adds the address of this operand address to a list of forward references associated with the address. SYMTAB entry.
→ When the definition for the symbol is encounted, scans, the reference list and inserts the address.
→ At the end of the program, reports the error if there are still SYMTAB entries indicated undefined symbols.

Two-pass assembleng:

The two pass assembler performs two passes over the source program.

In the first pass, it reads the entire source program, Looking only for label definitions. All the labels are collected, assigned address, and placed in the symbol table in this pass, no instructions as assebled and at the end the symbol table should contain all the labels defined in the program. To assign address to labels, the assembles maintains a location counter (LC).



05/

Ans to the Qus No: 01(C)

Ans: Cache Memory is a special high-speed memory. It is used to speed up and synchronize with high-speed CPU. Cache memory is costlier than main memory or disk memory but more economical than CPU registers.

Three levels of cache memory organization:

→ Level 1 or Register:

It is a type of memory in which data is stored and accepted that are immediately stored in CPU. Most commonly used register is accumulator, Program counter, address register eet etc.

→ Level 2 or Cache memory:

It is the fastest memory which has faster access time where data is temporarily stored for faster access.

→ Level 3 or Main Memory:

It is memory on which computer works currently. It is small in size and once power is off no power is off data no longer stays in this memory.

06

Ans to the QUS NO: 02(a)

Ans: Memory address register:

In a computer, the memory address register (MAR) is the CPU register that either stores the memory address from which data will be fetched to the CPU registers, or the address to which data will be sent and stored via Systems bus.

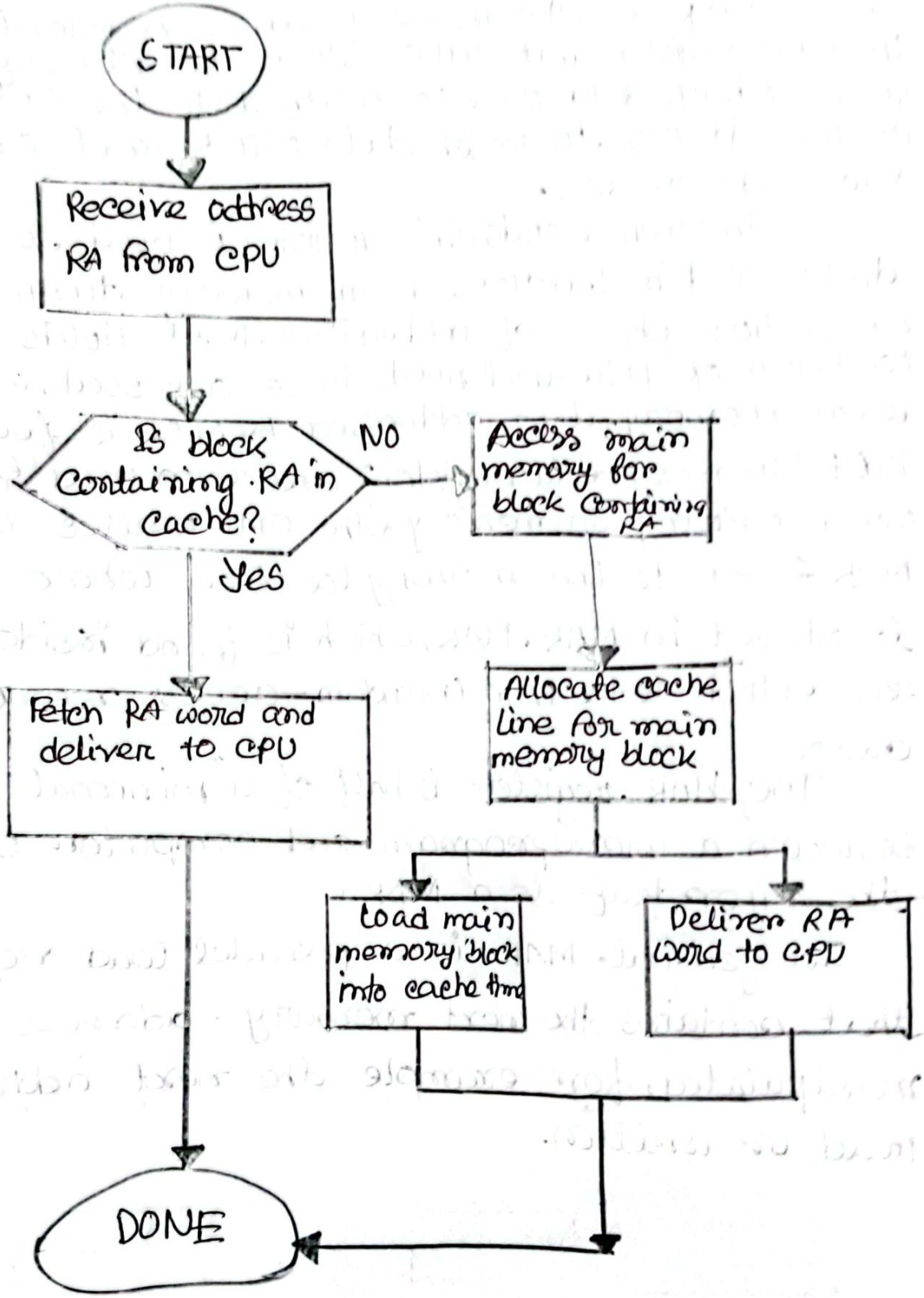
In other words, this register is used to access data and instructions from memory during the execution phase of instruction. MAR Holds the memory location of data that needs to be accessed. When reading form memory, data addressed by MAR is fed into the MDR (memory data register) and then used by the CPU. When writing to memory, the CPU writes data form MDR ~~from~~ to the memory location whose address is stored in MAR. MAR, which is found inside the CPU, goes either to the RAM (random-access memory) or cache.

The MAR register is half of a minimal interface between a microprogram and computer storage, the other half is a MDR.

In general, MAR is a parallel load register that contains the next memory address to be manipulated, for example the next address to be read or written.

Ans to the QUS NO 8 02 (5)

Ans: Cache Read operation:



08/

START Reciere address RA from CPU Ps block containing RA no access main memory for block containing RA ~~AA~~ M access ~~main~~ Yes Fetch RA word Allocate cache and deliver Line for main to CPU memory block boad main Deliver RA word memory block to CPU into cache Line DONE.