Victoria University of Bangladesh

Department computer Science & Engineering

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Program: B.Sc in CSE

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Batch: 22nd (Evening).

Course code: CSE-413.

Course Title: Microprocessor & Interfacing.

Mid-term Assessment

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Ans to the ques No - 1(a)

Block Diagram :

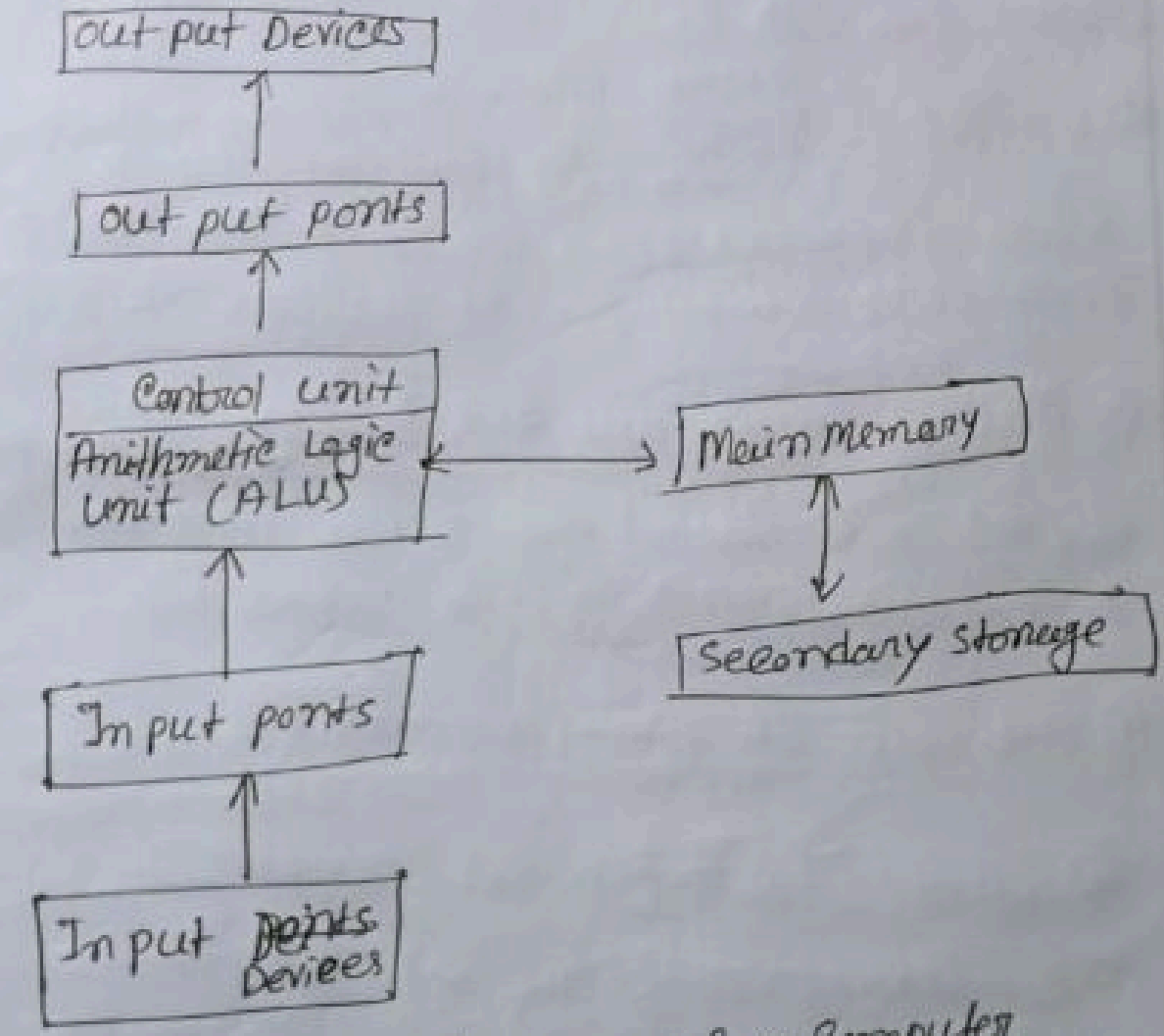

fig. Block diagram of a Computer

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Future of Microprocessor:

① Architecture: Microprocessors are available is 8 bit, 16 bit 32 bit, 64 bit architectures. The bit sizes can also be called bus with.

② parallel processing: The matticore chip that contains more than one processon in it, enables parallel processing at independent portions of a task.

③ Matti processing and time searing: The time is devided in to several eqol slices and it is allated to various processing is a roundtobin fashion.

④ Categories of micro processing:

ⓐ fedreed Instraction set Computer

ⓑ Complex Instraction set Computer

ⓒ Special purpose processors.

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Ans to the ques no 1 (B)

(c)

Bit manipulation instructions sets (BMI sets) are extensions to the x86 instruction set architecture for microprocessor from intel and AMD. the purpose of these instruction sets is to improve the speed of bit manipulation. All the instruction in these sets are non-SIMD and operate only on general-purpose registers.

There are two sets published by Intel: BMI and BMI2: they were both introduced with the Hasswell microarchitecture with BMI1 matching features offered by AMD's ABM instruction set and BMI2 extending them. Another two sets were published by AMD. ABM (Advanced Bit Manipulation which is also a subset of SSE 4a implemented by Intel as part of SSE 4.2 and BMI1), and TBM (Trailing Bit Manipulation. ant extension. introduced with piledriver based process are as an extension to BMI, but dropped again in for bulldozer based processors).

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Ans to the ques No 1 (c)

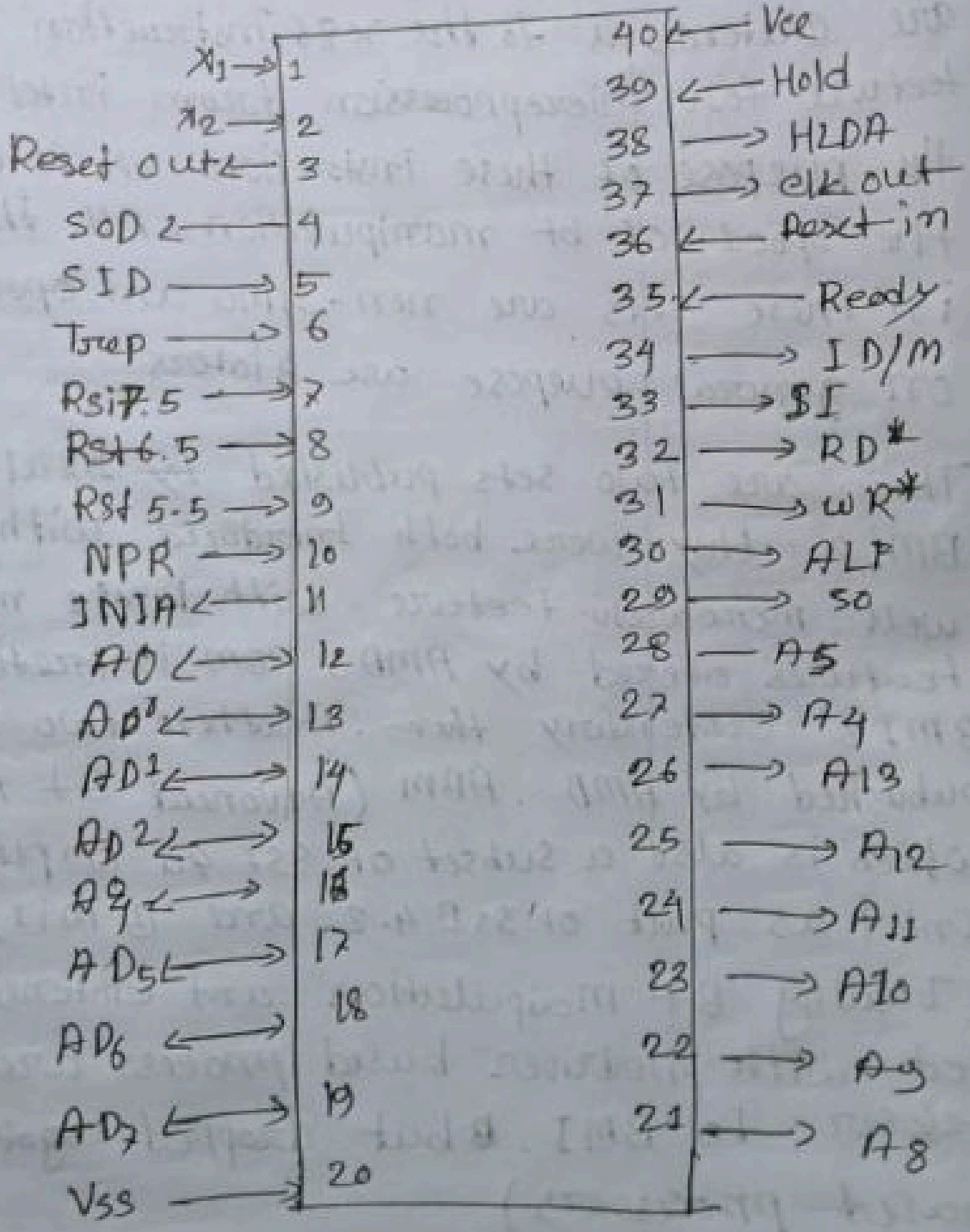

Fig. Pin diagram of 8085

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Ans to the Ques No-2(a)

Initially when any device has to send data between the device and the memory, the between has to seid DMA request to DMA Controller. The DMA Controller Sends Hold request to the cpu and waits for the cpu to assert the HLDA.

Ans to the ques No-2(b)

Features to 8257:

(a) It has four channels which can be used over four I/O devices.
(b) Each channel has 16 bit address and 14 bit counter.
(c) Each channel can transfer data upto 64 KBit.
(d) Each channel can be programmed independently.
(e) Each channel can perform read transfer, write transfer and Verify transfer operations.
(f) It generates MARK signal to the peripheral device that 128 bytes have been transferred.
(g) It requires a single phase clock.
(h) Its frequency flones from 200 H_z to 3 MH_z.

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① It operates in 2 modes, master mode and slave mode.

These are the main features of 8257 pin description. These things are very important for any 8257 pin description.

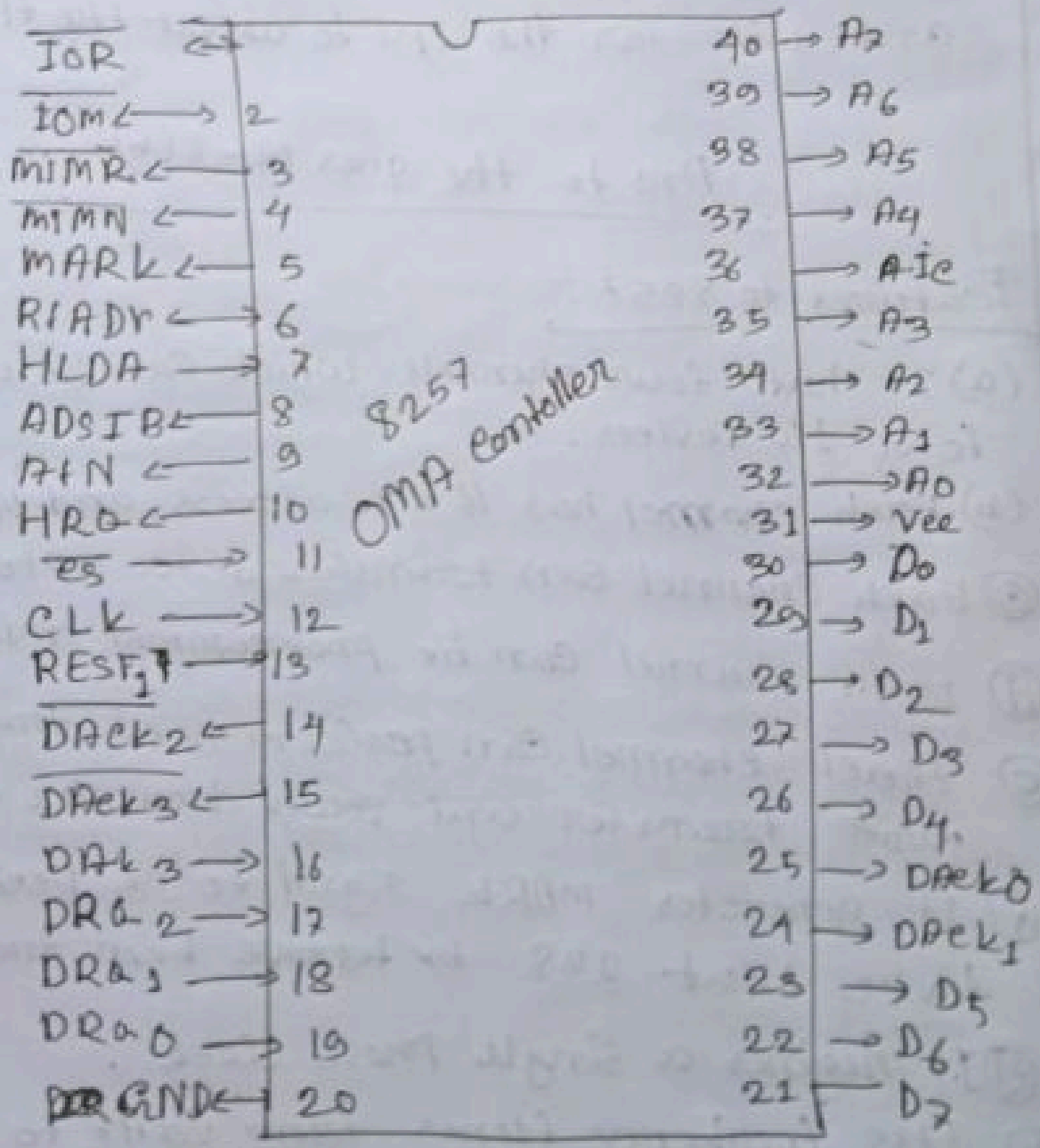

Fig. Pin diagram of 8257.

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