Victoria University of Bangladesh
Name: Md. Ziaul Hoque “Sohel”
Student ID: 2221220031
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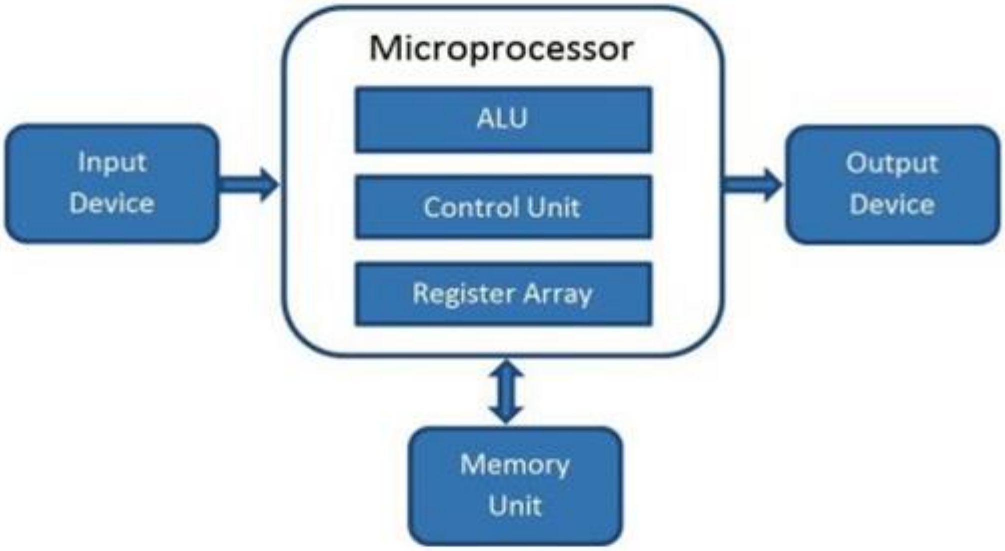
Answer to the Question No 1 (A)

Microprocessor:

Computer's Central Processing Unit (CPU) built on a single Integrated Circuit (IC) is called a microprocessor. A digital computer with one microprocessor which acts as a CPU is called microcomputer. It is a programmable, multipurpose, clock -driven, register-based electronic device that reads binary instructions from a storage device called memory, accepts binary data as input and processes data according to those instructions and provides results as output.

The microprocessor contains millions of tiny components like transistors, registers, and diodes that work together.

A microprocessor consists of an ALU, control unit and register array. Where ALU performs arithmetic and logical operations on the data received from an input device or memory. Control unit controls the instructions and flow of data within the computer. And, register array consists of registers identified by letters like B, C, D, E, H, L, and accumulator.



Answer to the Question No 1 (B)

8085 Architecture:

Intel 8085 is an 8-bit, NMOS microprocessor designed by Intel in 1977.

It has following configuration:

- It is a 40 pin I.C. package fabricated on a single LSI chip.
- The Intel 8085 uses a single +5Vd.c. supply for its operation.
- Intel 8085?s clock speed is about 3 MHz; the clock cycle is of 320ns.
- 8 ?bit data bus.
- Address bus is of 16-bit, which can address up to 64KB
- 16-bit stack pointer
- 16 bit PC (Program Counter)
- Six 8-bit registers are arranged in pairs :BC, DE, HL

Intel 8085 is used in mobile phones, microwave ovens, washing machines etc.

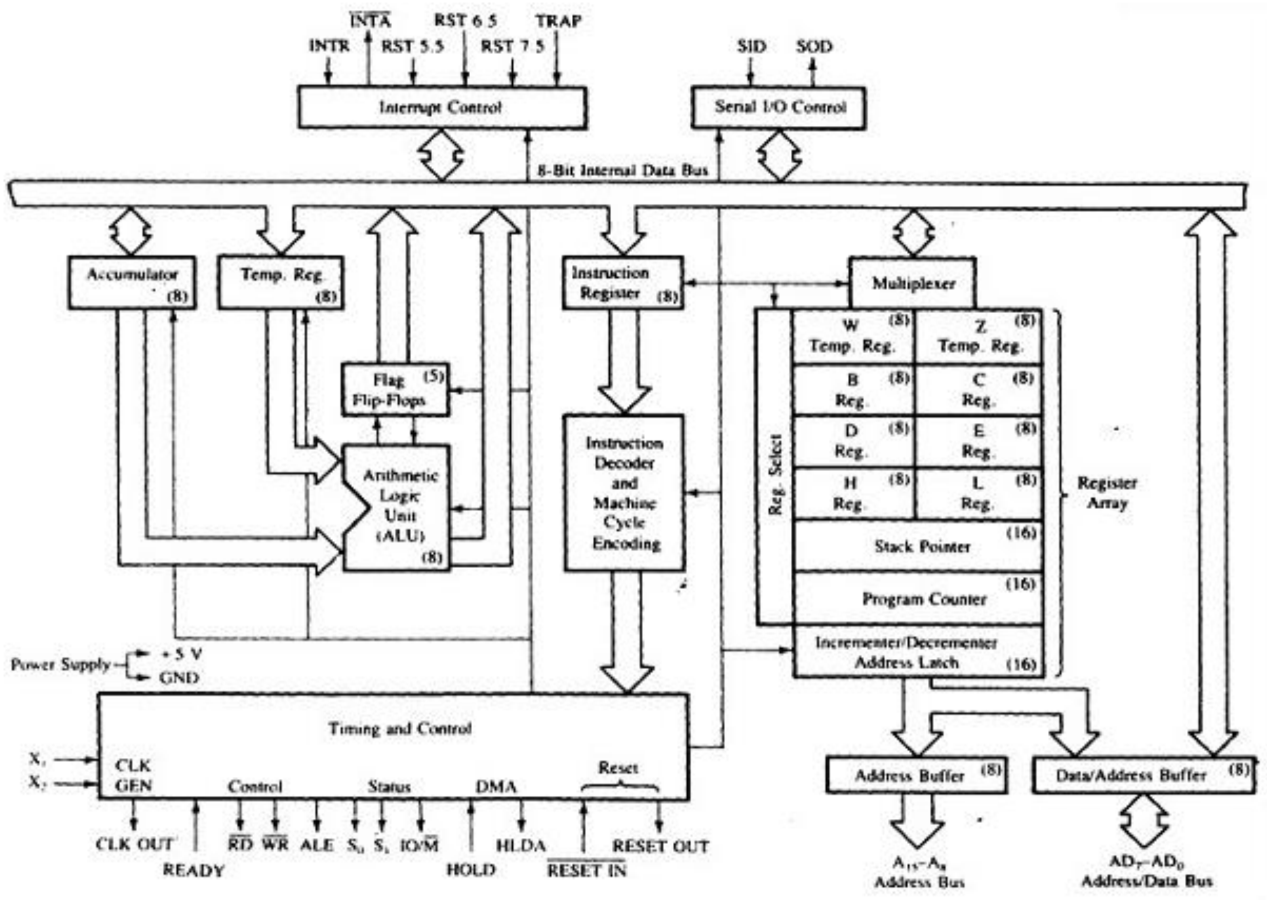


Fig: 8085 Architecture

Answer to the Question No 1 (C)

Bit Manipulation Instructions:

The Bit Manipulation Instructions in 8086 or Logical Instructions are

- **NOT**
- **AND**
- **OR**
- **XOR**

NOT Instruction: NOT destination. The NOT instruction inverts each bit of a byte or a word. The destination can be register or a memory location.

AND Instruction: AND destination, source. This instruction logically ANDs each bit of the source byte or word with the corresponding bit in the destination and stores result in the destination. The source may be an immediate number, a register or a memory location. The destination may be a register or a memory location. The source and destination both cannot be memory locations in the same instruction. The CF and OF are both 0 after AND. The PF, SF and ZF are affected. AF is undefined.

OR Instruction: OR destination, source. This instruction logically ORs each bit of the source byte or word with the corresponding bit in the destination and stores result in the destination. The source may be an immediate number, a register or a memory location. The destination may be a register or a memory location. The source and destination both can't be memory locations in the same instruction. The CF and OF are both 0 after OR. The PF, SF and ZF are affected. AF is undefined.

XOR Instruction: XOR destination, source.

This instruction logically XORs each bit of the source byte or word with the corresponding bit in the destination and stores result in the destination. The source may be an immediate number, a register or a memory location. The destination may be a register or a memory location. ⁻The source and destination both cannot be memory locations in the same instruction. The CF and OF are both 0 after XOR. The PF, SF and ZF are affected. AF is undefined.

TEST Instruction: TEST destination, source.

This Bit Manipulation Instructions in 8086 ANDs the contents of a source byte or word with the contents of the specified destination word. Flags are affected. But neither operand is changed. PF, SF and ZF will be updated to show the results of the ANDing. PF has meaning only for the lower 8 bits of the destination. AF will be undefined.

Answer to the Question No 2 (A)

DMA Operations:

Following is the sequence of operations performed by a DMA –

- Initially, when any device has to send data between the device and the memory, the device has to send DMA request (DRQ) to DMA controller.
- The DMA controller sends Hold request (HRQ) to the CPU and waits for the CPU to assert the HLDA.
- Then the microprocessor tri-states all the data bus, address bus, and control bus. The CPU leaves the control over bus and acknowledges the HOLD request through HLDA signal.
- Now the CPU is in HOLD state and the DMA controller has to manage the operations over buses between the CPU, memory, and I/O devices.

Answer to the Question No 2 (B)

8257 Pin Diagram:

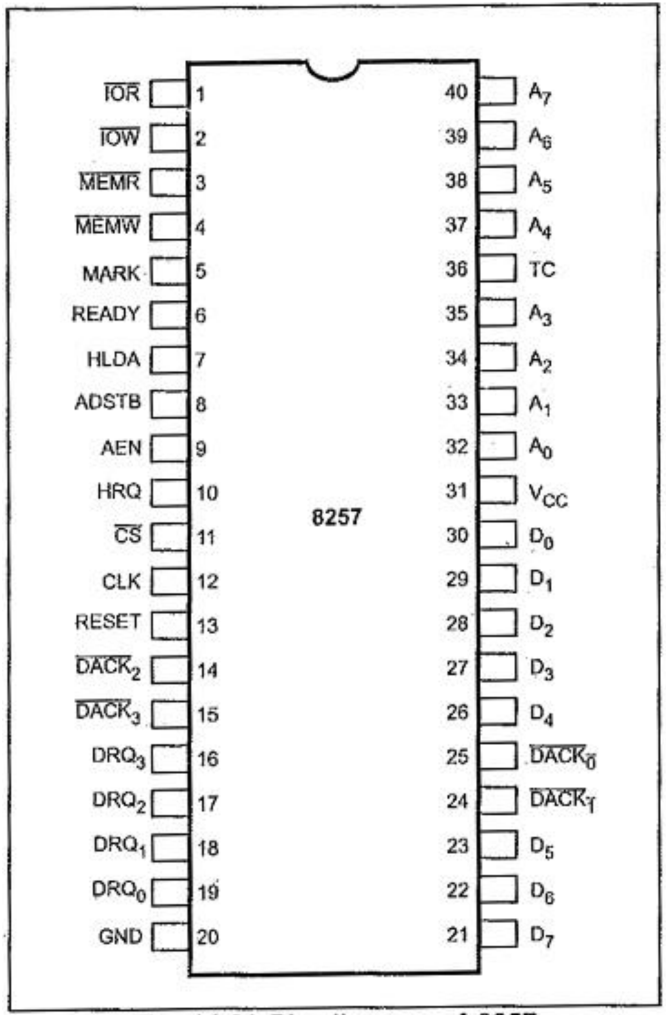


Fig. 14.61 Pin diagram of 8257

8257 Pin Description:

Address Bus (A_0-A_3 and A_4-A_7): The four least significant lines A_0-A_3 are bi – directional tri – state signals. In the idle cycle they are inputs and used by the CPU to address the register to be loaded or read. In the Active cycle they output the lower 4 bits of the address for DMA operation. A_4-A_7 are unidirectional lines, provide 4-bits of address during DMA service.

Address Strobe (ADSTB): This signal is used to demultiplex higher byte address and data using external latch.

Address Enable (AEN): This active high signal enables the 8-bit latch containing the upper 8-address bits onto the system address bus. AEN can also be used to disable other system bus drivers during DMA transfers.

Memory Read and Memory Write (MEMR, MEMW): These are active low tri-state signals. The MEMR signal used to access data from the addressed memory location during a DMA read or memory-to-memory transfer and MEMW signal is used to write data to the addressed memory location during DMA write or memory to memory transfer.

I/O Read and I/O Write (IOR and IOW): These are active low bi-directional signals. In idle cycle, these are an input control signals used by CPU to read/write the control registers. In the active cycle IOR signal is used to access data from a peripheral and IOW signal is used to send data to the peripheral.

Chip Select (CS): This is an active low input, used to select the 8257 as an I/O device during the idle cycle. This allows CPU to communicate with 8257 Pin Diagram.

Reset: This active high signal clears, the command, status, request and temporary registers. It also clears the first/last flip-flop and sets the Master Register. After reset the device is in the idle cycle.

Ready: This input is used to extend the memory read and write signals from the 8257 to interface slow memories or I/O devices.

Hold request (HRQ): Any valid DREQ causes 8257 to issue the HRQ. It is used for requesting CPU to get the control of system bus.

Hold Ackmiwledge (HLDA): The active high Hold Acknowledge from the CPU indicates that it has relinquished control of the system bus.

$DREQ_0$-$DREQ_3$: These are DMA request lines, which are activated to obtain DMA service, until the corresponding DACK signal goes active.

$DACK_0$-$DACK_3$: These are used to indicate peripheral devices that the DMA request is granted.

Terminal Count (TC): This is active high signal concern with the completion of DMA service. The TC output signal is activated at the end of DMA service, i.e. when present cycle is a last cycle for the current data block.

MARK: This output notifies the selected peripheral that the current DMA cycle is the 128th cycle since the previous MARK output. MARK always occurs at 128 (all multiplies of 128) cycles from the end of the data block.

END