Victoria University
of Bangladesh

MID Term Assessment

Md Bakhtiar Chowdhury

ID: 2121210061

Department: CSE

Semester: Fall -2022

Batch: 21th

Course Title: Microprocessor

Course Code: CSE 413

Submitted To:

Umme Khadiza Tithi

Lecturer, Department of Computer Science & Engineering

Victoria University of Bangladesh

Submission Date: 15 December, 2022

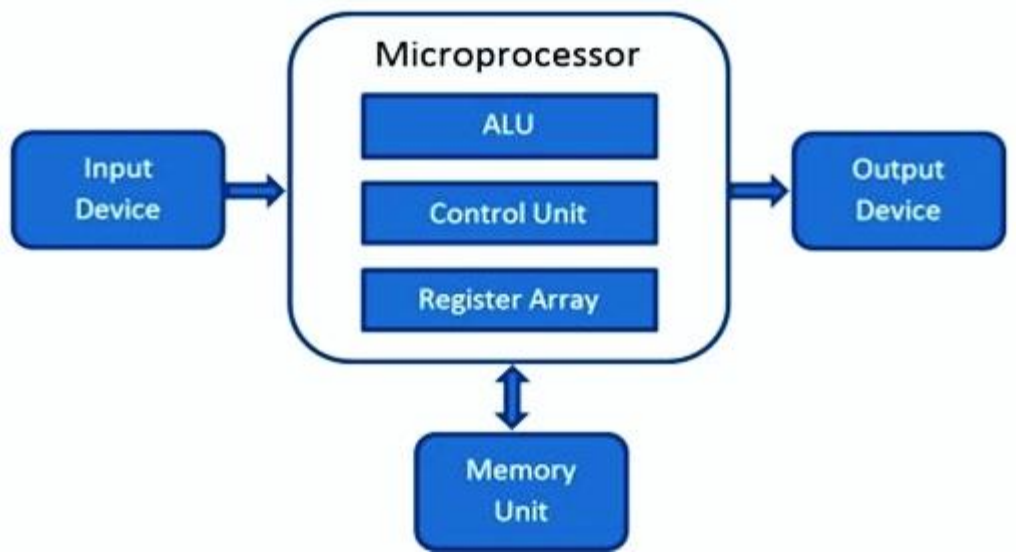
ID- 2121210061, Name: Md Bakhtiar Chowdhury, Program: BSc in CSE (R)

Course Code: CSE 413, Course Title: Microprocessor

Answer to the question no 1(a)

Write down Block Diagram of a basic Microcomputer and features Of Microprocessor ?

Block Diagram of a basic Microcomputer:



A microprocessor consists of an ALU, control unit and register array. Where ALU performs arithmetic and logical operations on the data received from an input device or memory. Control unit controls the instructions and flow of data within the computer. And, register array consists of registers identified by letters like B, C, D, E, H, L, and accumulator.

Features of Microprocessor: Microprocessor is used in a variety of applications due to their unique features such as size, weight, cost, high computing power, and low power consumption, etc., Microprocessor fitted systems are used.

- to monitor and control operations of Industrial devices by measuring key parameters like temperature, pressure, speed.
- in instruments to raise an alert or warning on extreme conditions.

- to automate office work/business processes and improve white collar productivity.
- in simplifying publishing activity.
- to speed up the information exchange through Telephone and Satellite network.
- in rolling out innovations in entertainment, games and Photography.
- to make everybody and everything stay connected with each other.
- **Low Cost** - Due to integrated circuit technology microprocessors are available at very low cost. It will reduce the cost of a computer system.
- **High Speed** - Due to the technology involved in it, the microprocessor can work at very high speed. It can execute millions of instructions per second.
- **Small Size** - A microprocessor is fabricated in a very less footprint due to very large scale and ultra large scale integration technology. Because of this, the size of the computer system is reduced.
- **Versatile** - The same chip can be used for several applications, therefore, microprocessors are versatile.
- **Low Power Consumption** - Microprocessors are using metal oxide semiconductor technology, which consumes less power.
- **Less Heat Generation -** Microprocessors uses semiconductor technology which will not emit much heat as compared to vacuum tube devices.
- **Reliable** - Since microprocessors use semiconductor technology, therefore, the failure rate is very less. Hence it is very reliable.
- **Portable** - Due to the small size and low power consumption microprocessors are portable.

ID- 2121210061, Name: Md Bakhtiar Chowdhury, Program: BSc in CSE (R)

Course Code: CSE 413, Course Title: Microprocessor

Answer to the question no 1(b)

 # Draw 8085 Architecture ?

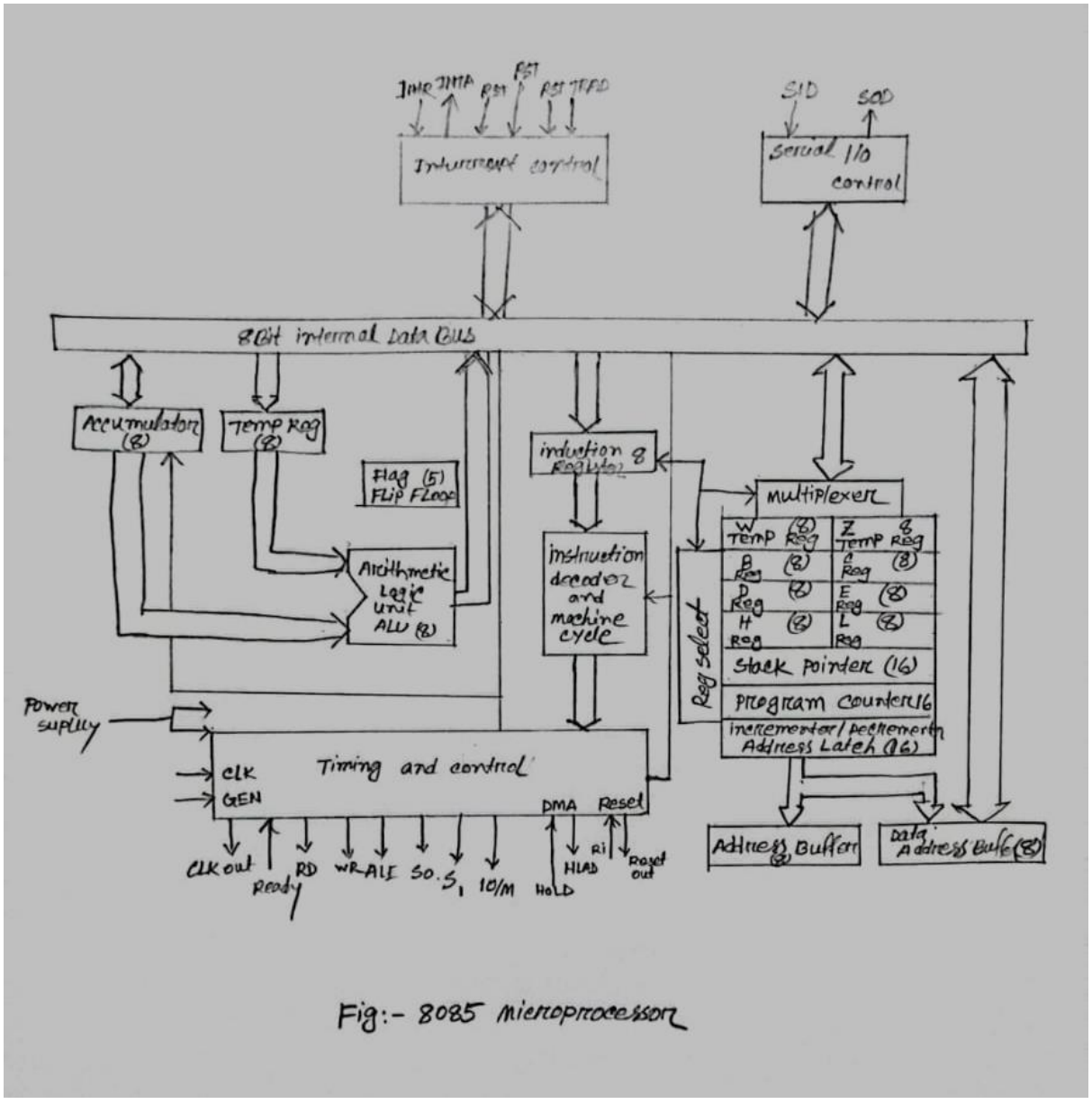


Fig:- 8085 Microprocessor

ID- 2121210061, Name: Md Bakhtiar Chowdhury, Program: BSc in CSE (R)

Course Code: CSE 413, Course Title: Microprocessor

Answer to the question no 1(c)

 # Define Bit Manipulation Instructions ?

Answer:

Bit Manipulation Instructions: These instructions are used to perform Bit wise operations.

Logical Instructions	Shift Instructions	Rotate Instructions
NOT	SHL/SAL	ROL
AND	SHR	ROR
OR	SAR	RCL
XOR		RCR
TEST		

When binary data are manipulated in a register or a memory location, the rightmost bit position is always numbered bit 0. Bit position numbers increase from bit 0 toward the left, to bit 7 for a byte, and to bit 15 for a word.

Logical Instructions: Logic operations provide binary bit control in low-level software. The logic instructions allow bits to be set, cleared, or complemented. Lowlevel software appears in machine language or assembly language form and often controls the I/O devices in a system. All logic instructions affect the flag bits. Logic operations always clear the carry and overflow flags, while the other flags change to reflect the condition of the result.

Mnemonic	Meaning	Format	Operation	Flags Effected
NOT	Logical NOT	NOT D	$(\overline{D}) \rightarrow (D)$	None
AND	Logical AND	AND D,S	$(S) .D) \rightarrow (D)$	O, S, Z, P, C
OR	Logical Inclusive OR	OR D,S	$(S) + D) \rightarrow (D)$	O, S, Z, P, C
XOR	Logical Exclusive OR	XOR D,S	$(S) \oplus D) \rightarrow (D)$	O, S, Z, P, C

Example: Set bit 7 of AX register ORAH, 80H ; (xxxxxxxxOR1000 0000 = 1xxxxxxx)

Shift instructions: Shift instructions position or move numbers to the left or right within a register or memory location. They also perform simple arithmetic such as multiplication by powers of 2+n (left shift) and division by powers of 2-n (right shift). The microprocessor's instruction set contains four different shift instructions: Two are logical shifts and two are arithmetic shifts.

Mnem.	Meaning	Format	Operation	Flags Effected
SAL/SHL	Shift arithmetic left /shift logical left	SAL D, Count SHL D,Count	Shift the (D) left by the number of bit positions equal to Count and fill the vacated bits positions on the right with zeros	C, P, S, Z A undefined O undefined if count ≠1
SHR	shift logical right	SHR D,Count	Shift the (D) right by the number of bit positions equal to Count and fill the vacated bit positions on the left with zeros	C, P, S, Z A undefined O undefined if count ≠1
SAR	Shift arithmetic right	OR D,S	Shift the (D) right by the number of bit positions equal to Count and fill the vacated bit positions on the left with the original most significant bit	C, P, S, Z A undefined O undefined if count ≠1

Example: Let AX=1234H what is the value of AX after execution of next instruction SHL AX,1

Rotate Instructions: Numbers rotate through a register or memory location, through the C flag (carry), or through a register or memory location only. With either type of rotate instruction, the programmer can select either a left or a right rotate. Addressing modes used with rotate are the same as those used with shifts. A rotate count can be immediate or located in register CL.

Mnem.	Meaning	Format	Operation	Flags Effected
ROL	Rotate left	ROL D, Count	Rotate the (D) left by the number of bit positions equal to Count.Each bit shifted out from the leftmost bit goes back into the rightmost bit position.	C O undefined if count ≠1
ROR	Rotate right	RORD,Count	Rotate the (D) right by the number of bit positions equal to Count. Each bit shifted out from the rightmost bit goes back into the leftmost bit position.	C, O undefined if count ≠1
RCL	Rotate left through carry	RCLD,Count	Same as ROL except carry is attached to (D) for rotation.	C , O undefined if count ≠1
RCR	Rotate right through carry	RCRD,Count	Same as ROR except carry is attached to (D) for rotation.	C , O undefined if count ≠1

Example: Assume AX = 1234H, what is the result of executing the instruction ROL AX, 1

Answer to the question no 2(a)

 # How DMA operations are Performed ?

Answer:

DMA stands for Direct Memory Access. It is designed by Intel to transfer data at the fastest rate. It allows the device to transfer the data directly to/from memory without any interference of the CPU.

Using a DMA controller, the device requests the CPU to hold its data, address and control bus, so the device is free to transfer data directly to/from the memory. The DMA data transfer is initiated only after receiving HLDA signal from the CPU.

Following is the sequence of operations performed by a DMA−

- Initially, when any device has to send data between the device and the memory, the device has to send DMA request (DRQ) to DMA controller.

- The DMA controller sends Hold request (HRQ) to the CPU and waits for the CPU to assert the HLDA.
- Then the microprocessor tri-states all the data bus, address bus, and control bus. The CPU leaves the control over bus and acknowledges the HOLD request thro ugh HLDA signal.
- Now the CPU is in HOLD state and the DMA controller has to manage the operations over buses between the CPU, memory, and I/O devices.

Answer to the question no 2(b)

 # Define 8257 pin Description ?

Answer:

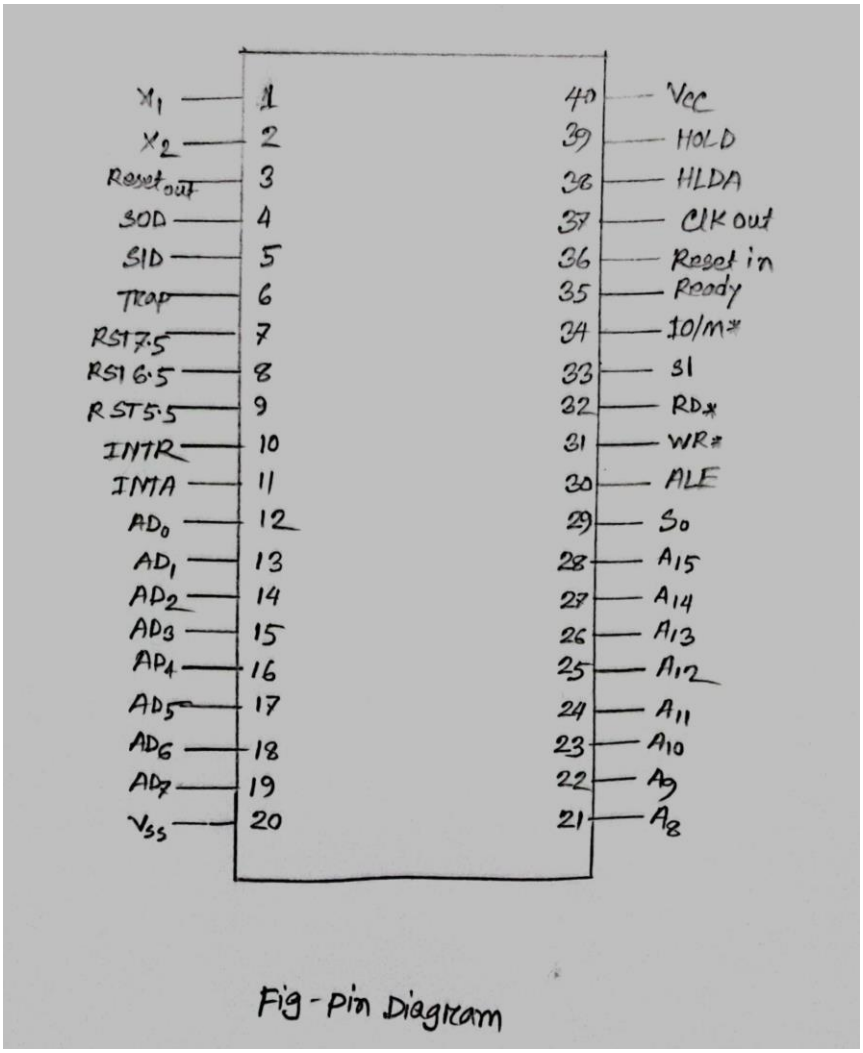


Fig - Pin Diagram

DRQ_0–DRQ3

These are the four individual channel DMA request inputs, which are used by the peripheral devices for using DMA services. When the fixed priority mode is selected, then DRQ_0 has the highest priority and DRQ_3 has the lowest priority among them.

$DACK_o$ – $DACK_3$

These are the active-low DMA acknowledge lines, which updates the requesting peripheral about the status of their request by the CPU. These lines can also act as strobe lines for the requesting devices.

D_o – D_7

These are bidirectional, data lines which are used to interface the system bus with the internal data bus of DMA controller. In the Slave mode, it carries command words to 8257 and status word from 8257. In the master mode, these lines are used to send higher byte of the generated address to the latch. This address is further latched using ADSTB signal.

IOR

It is an active-low bidirectional tri-state input line, which is used by the CPU to read internal registers of 8257 in the Slave mode. In the master mode, it is used to read data from the peripheral devices during a memory write cycle.

IOW

It is an active low bi-direction tri-state line, which is used to load the contents of the data bus to the 8-bit mode register or upper/lower byte of a 16-bit DMA address register or terminal count register. In the master mode, it is used to load the data to the peripheral devices during DMA memory read cycle.

CLK

It is a clock frequency signal which is required for the internal operation of 8257.

RESET

This signal is used to RESET the DMA controller by disabling all the DMA channels.

A_0 - A_3

These are the four least significant address lines. In the slave mode, they act as an input, which selects one of the registers to be read or written. In the master mode, they are the four least significant memory address output lines generated by 8257.

CS

It is an active-low chip select line. In the Slave mode, it enables the read/write operations to/from 8257. In the master mode, it disables the read/write operations to/from 8257.

A_4 - A_7

These are the higher nibble of the lower byte address generated by DMA in the master mode.

READY

It is an active-high asynchronous input signal, which makes DMA ready by inserting wait states.

HRQ

This signal is used to receive the hold request signal from the output device. In the slave mode, it is connected with a DRQ input line 8257. In Master mode, it is connected with HOLD input of the CPU.

HLDA

It is the hold acknowledgement signal which indicates the DMA controller that the bus has been granted to the requesting peripheral by the CPU when it is set to 1.

MEMR

It is the low memory read signal, which is used to read the data from the addressed memory locations during DMA read cycles.

MEMW

It is the active-low three state signal which is used to write the data to the addressed memory location during DMA write operation.

ADST

This signal is used to convert the higher byte of the memory address generated by the DMA controller into the latches.

AEN

This signal is used to disable the address bus/data bus.

TC

It stands for 'Terminal Count', which indicates the present DMA cycle to the present peripheral devices.

MARK

The mark will be activated after each 128 cycles or integral multiples of it from the beginning. It indicates the current DMA cycle is the 128th cycle since the previous MARK output to the selected peripheral device.

V_{cc}

It is the power signal which is required for the operation of the circuit.

>>>>>>END<<<<<<