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8th Batch (CSE - Evening)
Subject: computer Architecture
code: CSE - 313

Ans to the Q: No: - 01 (a)

(a)

Ans: Describing the possible Organization of Embedded System:

As its name suggests, Embeded means Something that is attached to another thing. An Embedded system can be a Part of a large system in Hardware system having Software Embedded unit. An embedded system is a Micro controller of Microprossesor based system which is designed to performa Specific task. for example a fire Alarm is an Embedded system. It will Sence only smoke.

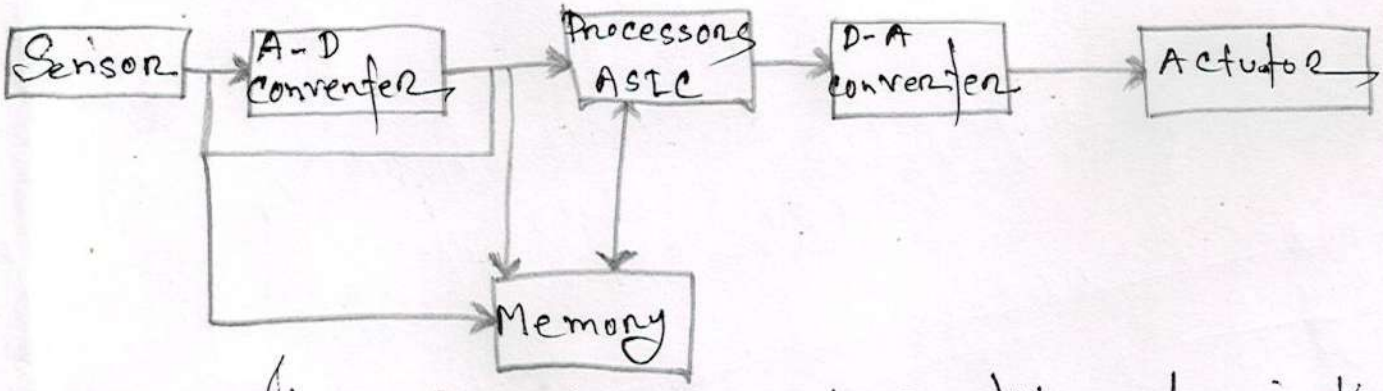
An Embedded system has Three Components :-

* (1) It has application software.
* (2) It has hardwere.
* (3) It has real time operating system (RTOS).

That application software an provide mechanism to let the prossesor run a prosses as per scheduling by following a plan to control the latencies.

#(1)(a) → Basic structure of an Embedded System:

The following illustration shows the basic structure of an Embedded system:-



Sensor: It measures the physical quantity and converts it to an electrical signal which can be ready by an observer or by any Electronic instrument like an A2D Converter. It's a measured quantity to the memory.

A-D Converter: An analog to digital converter converts the Analog signal send by the sensor into a digital signal.

Processor's ASIC: Processors Prosses the data to mesure the output and store into the memory.

D-A convertor: A digital to Analog converter converts the digital data fed by the processor to analog Data.

Actuator: A Actuator compares the output given by the D-A converter to the actual (Expected) Output the stored inito and stors the Approved Output.

Ans to the Q:NO:1 - (b)

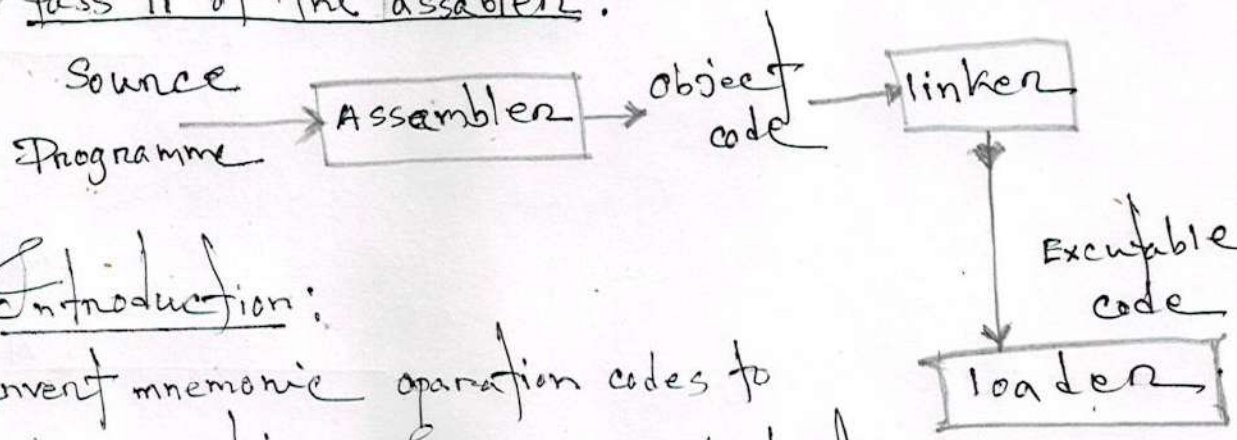
(b) Ans: Drawing the pass One and two in a two-pass assembler:

Pass 1 of the assembler: Data structure used in pass 1

1. OPIA
2. SYMTAB
3. LITTAB
4. POOLTAB.

Algorithm - Intemediate code - Declaration and Assembler Directive - Processing.

Pass II of the assabler:



Introduction:

Convert mnemonic operation codes to their machine Language Equivalents.

Convert symbolic operands to their equivalent machine Address

Build the machine instruction in the proper format.

Convert the Data constant to internal machine representation.

Write the object programme and the assembly listing.

1(b) Two pass Assembler Diagram:-

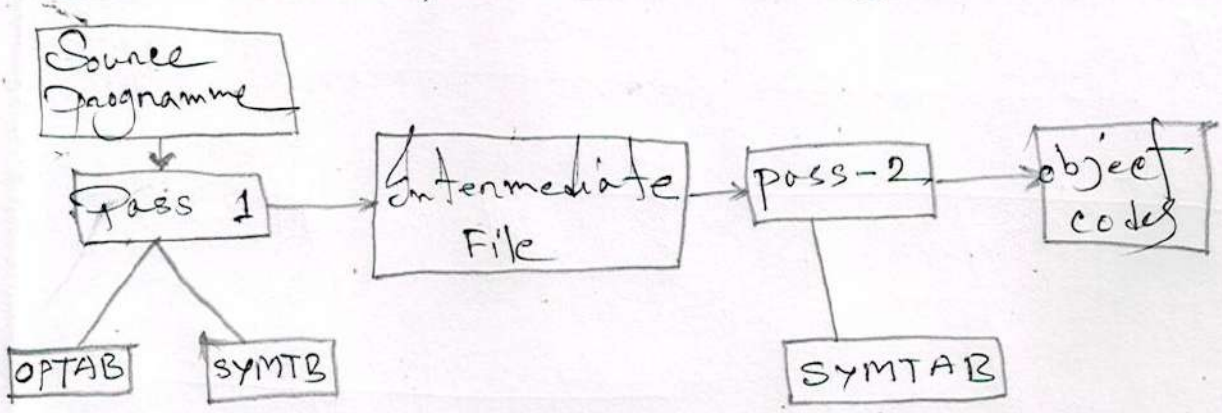


Fig: Two pass Assembler.

Pass 1: 1. Separate the symbol, Mnemonic opcode, and operand fields.
2. Build the symble table.
3. Perform LC processing.
4. Contruct Intermediate Representation.

Pass 2: Synthesize the teraget Programme.

Advanced Assembler Directives.

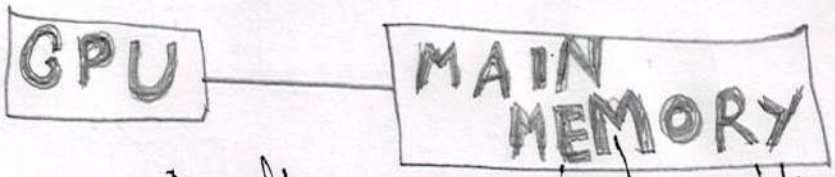
⇒ Origin.
⇒ EQU.

Ans: to the Q: NO! - (1) - (C)

(c) Three Level cache Organization:

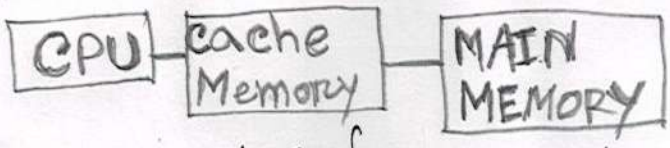
Cache is random Access memory used by the cpu to reduce the Avarage time taken to Access Memory.

Case 1: System Design with out cache memory:



Here the cpu Directly communicates with the main memory and no caches are invalved. In this case, the cpu needs to Accass the main memory 10 times to Access the desired Information.

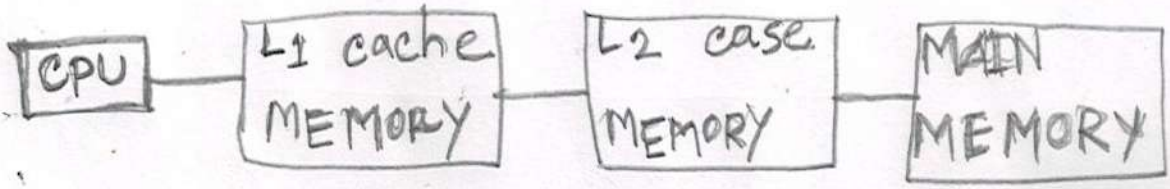
Case 2: system design with cach memory:



Here the CPU at first checks whether the desired data is present in the case memory or not i.e. whether there is a "hit" in cache or "Miss" in the cache. Suppose there is 8 Miss in cache memory. then the main memory will be Accessed Only 8 times. we can see that the main memory is reduced. Beeuse the main Memory is accessed a lesser number of times then that in the previous case.

1(c)

case (3): System Design with Multi level cache Memory:



→ Here the case performance is optimized furthure by introducing multilevel cases. As soon in the above figure we are concidaring 2 Lavel case desing. Suppose there is 3 Missin the L1 cache mamory and out of this 3 missed there is 2 miss in the L2 cashe memory then the main memory will be accessed only 2 times. It is clear that Here the miss menalty is Reduced considerably than that in the Proriovs case there by improving the performance of cache memory.

Ans: to the Q: No: 2(a)

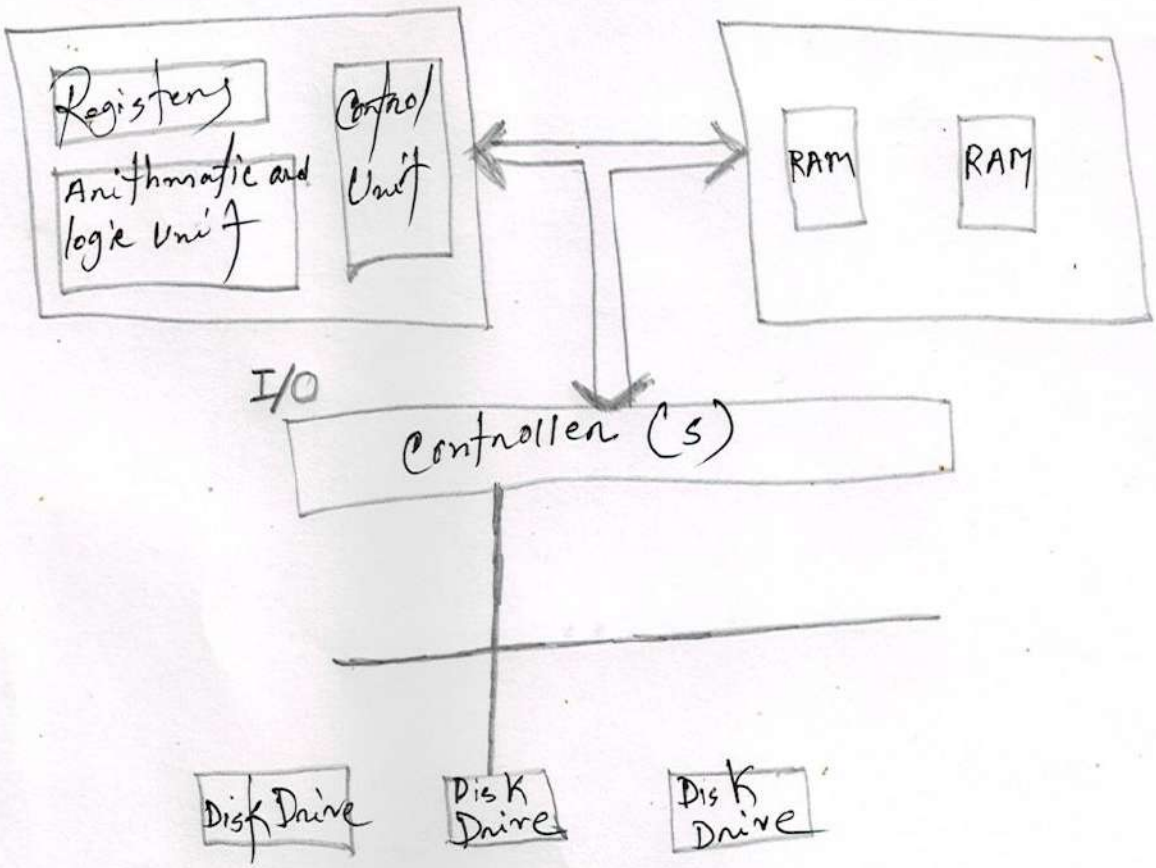
(a)

Ans: Memory Access Register:

(i) This is an architechire that is led by Instruction so that Operations are performed on the memory and the register. If architostrure has all the operents the register. It is called as register plus memory architacture.

(ii) One of the Operents of an Operation can be in the memory and the other one in the register. This acts as a difference form others in the register or in the memory.

(iii) Example are IBM system/360 and Intel x86.



(2) (a)

Registers are small in size and the number are also less in cpu. The size of a register in less then 64 bits. It is faster then the main memory and disk memory.

The word size depends on the size of General Registers.

⇒ Type and function of Register memory.

- Memory Address Register
- Memory Buffer Register
- Instruction Register
- Programme counter Register
- Accumulator Register
- Stack controler Register
- Flag Register.

Ans to the Q. No (2) (b)

(b) Draw the cache read Operation;

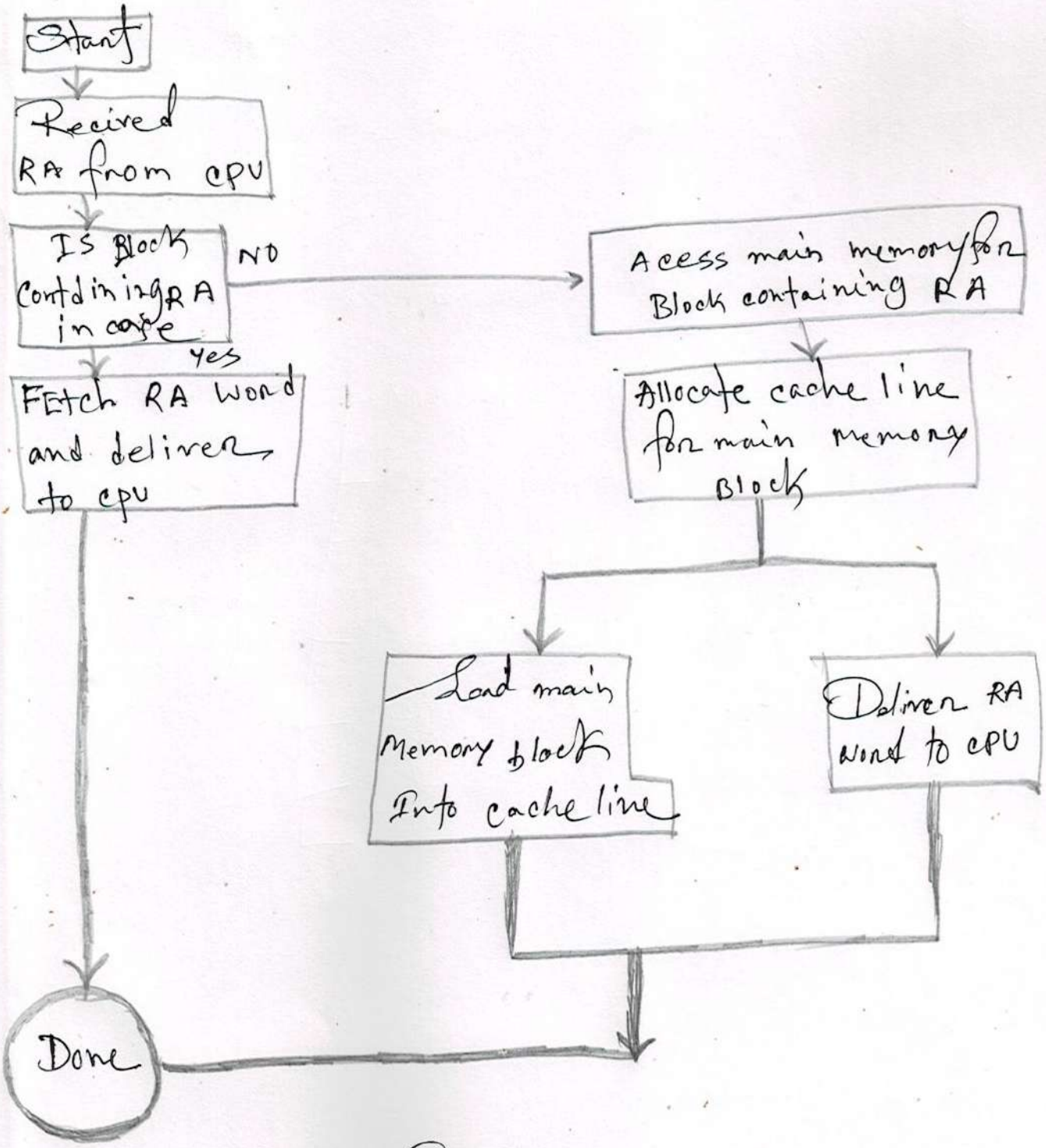


Figure: Cache Read Operation.