Mid Assessment

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CSE, 21st Batch

Computer Architecture

Course Code: CSE-313

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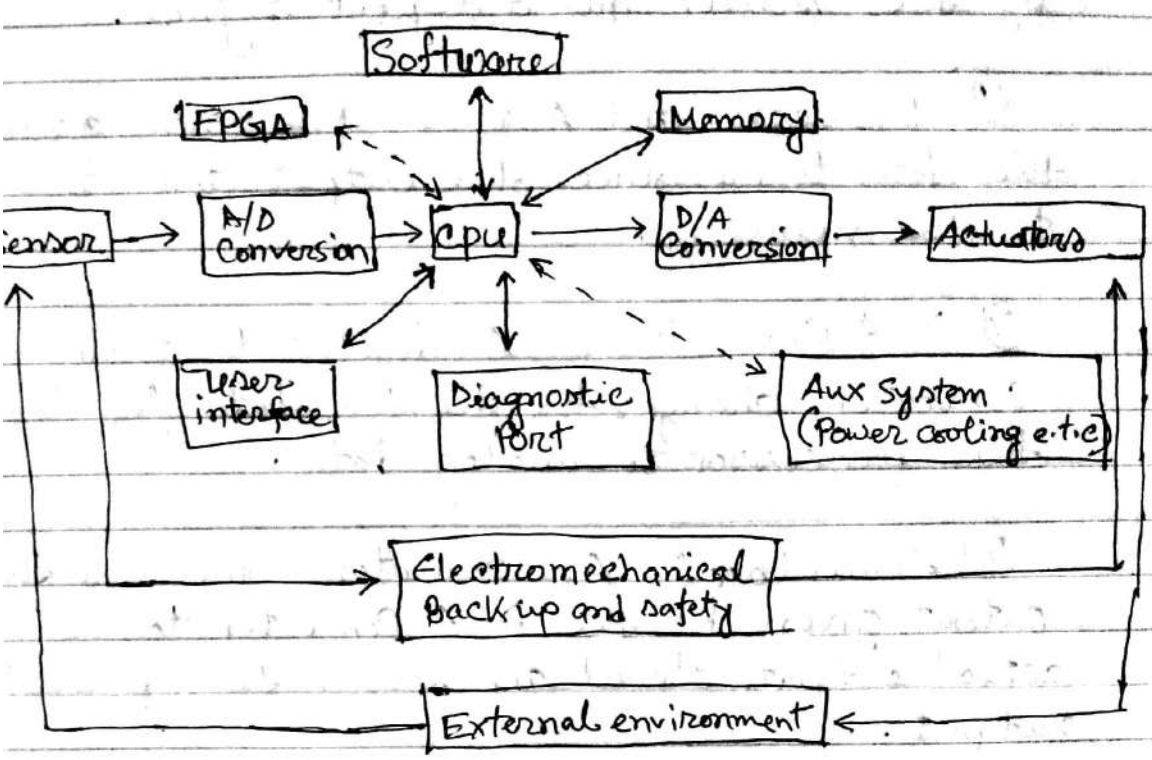
Answer to the Q. no - 01(a)



(Organized Embedded System)

* Structure of an embedded System :-

The basic structure of embedded System includes the following components -

(1) Sensor :- The sensor measures the and converts the physical quantity to an electrical signal, which can then be ready by an embedded systems engineer or any electronic instrument. A sensor stores the measured quantity to the memory.

(2) A-D Converter :- An analog to digital converter converts the analog signal sent by the sensor into a digital signal.

(3) Processor and ASICs :- processor asses the data to measure the output and store it to the memory.

(4) D-A Converter :- A digital to analog converter changes the digital data fed by the processor to analog data.

(5) Actuator :- An actuator compares the output given by the D-A Converter to the actual output stored and stores the approved output.

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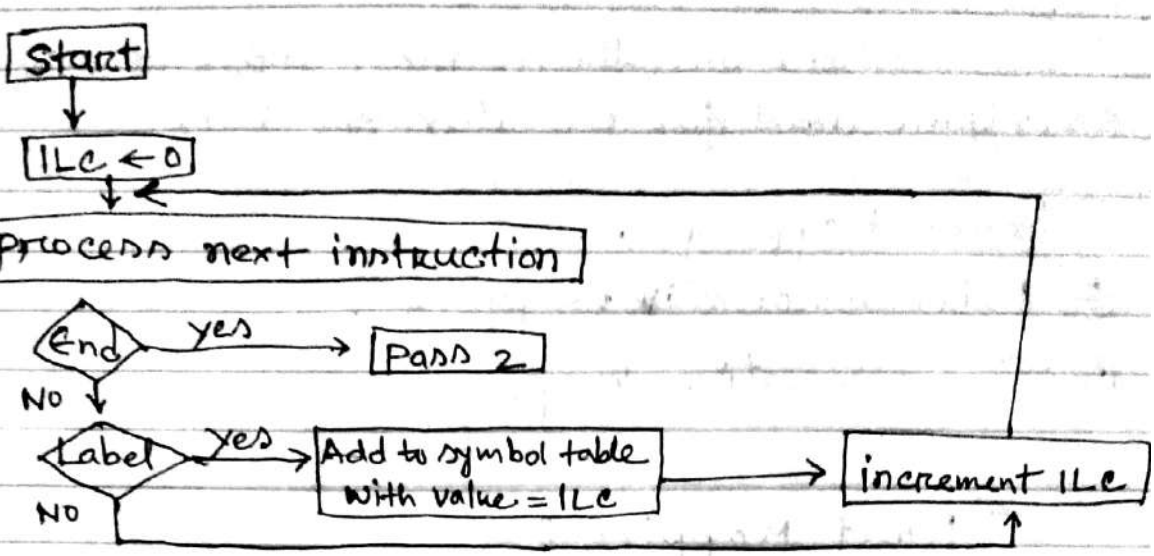
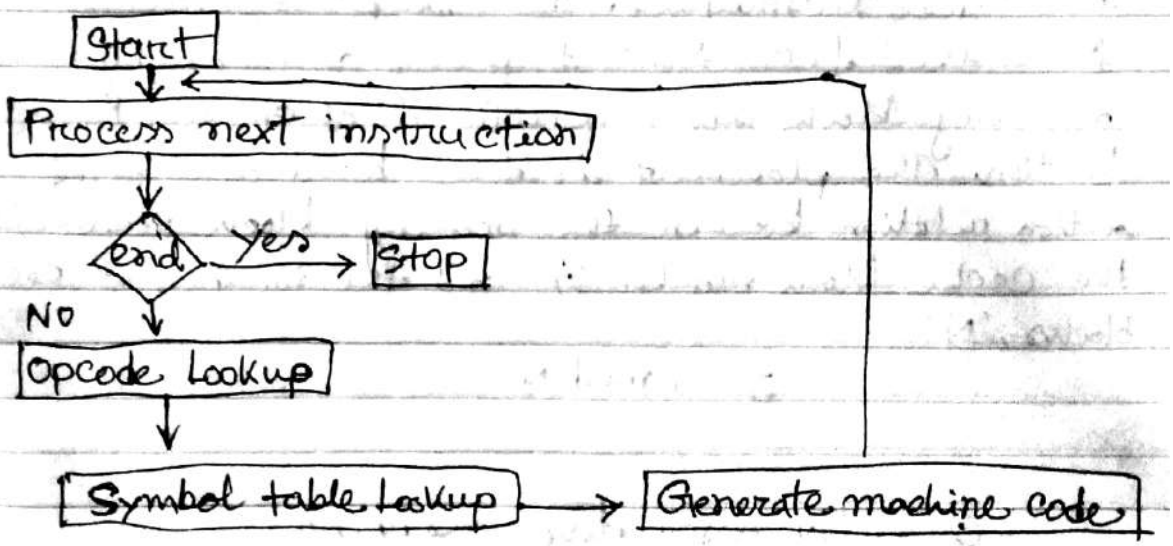
Ans. to the Q. no - 1(b)

* Simplified pass one in a two pass assembler :-



* Simplified Pass two in a two pass assembler :-



Ans to the q.no - 1(c)

Cache memory organization :-

There are three main different organiz techniques used for are discussed below -

1. Direct Mapping.
2. Fully associative mapping.
3. Set associative mapping.

(1) Direct Mapping :-

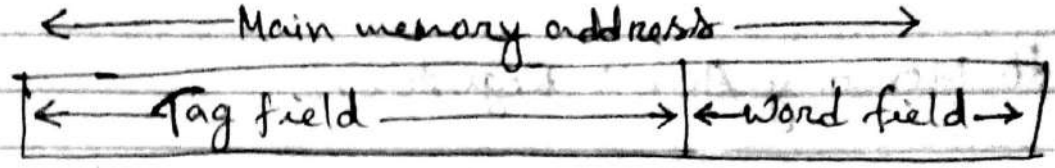
This is the simplest among the three techniques. It's simplicity stems from the fact that it places an incoming main memory block into a specific fixed cache block's location. The placement is done based on a fixed location relation between the incoming block number, 'i' the cache block number, 'j' and the number of cach blocks, 'N'

$$j = i \bmod N$$

(2) Fully associative mapping :-

According to this technique, an incoming main memory block can be placed in any available cache block. Therefore the address issued by the processor need only have two fields. These are the 'tag' and 'word' field. The first uniquely identifies the element within the block that is

requested by the processor.



① Word field = $\log_2 B$, where B is the size of block in words.

② Tag field = $\log_2 M$, where M is the size of main memory in blocks

③ The number of bits in the main memory address = $\log_2(B \times M)$

③ Set Associative Mapping :-

In this technique, the cache is divided into a number of sets. Each set consists of a number of blocks. $S = i \bmod S$ where 'S' is the number of sets in the cache, 'i' is the main memory block number, and 'S' is the specific cache set which block 'i' maps. The address issued by the processor is devided into three distinct fields - 'Tag', 'set' and 'word field'.

① Word field = $\log_2 B$, 'B' is the size of the block in words.

② Set field = $\log_2 S$, 'S' is the number of sets in the cache.

③ Tag field = $\log_2 (M/S)$, M = size of main memory blocks.
$S = N/B_s$, where N is the number of cache blocks and B_s is the number of blocks per set.

④ The number of bits in the main memory address = $\log_2(B \times M)$

Ans. to the Q.no - 2(a)

Memory Access Registers :—

Two registers are essential in memory - write and read operations : the memory data register (MDR) and memory address register (MAR) are used exclusively by the CPU and are not directly accessible to programmers.

In order to perform a write operation into a specified memory location, the MDR and MAR are used as follows —

① The word to be stored into the memory location is first loaded by the cpu into MDR.

② The address of the location into which the word is to be stored is loaded by the cpu into a MAR.

③ A write signal is issued by the cpu.

⇒ Similarly, to perform a memory read operation the MDR and AMR are used as follows —

① The address of location from which the word is to be read is loaded into the MAR.

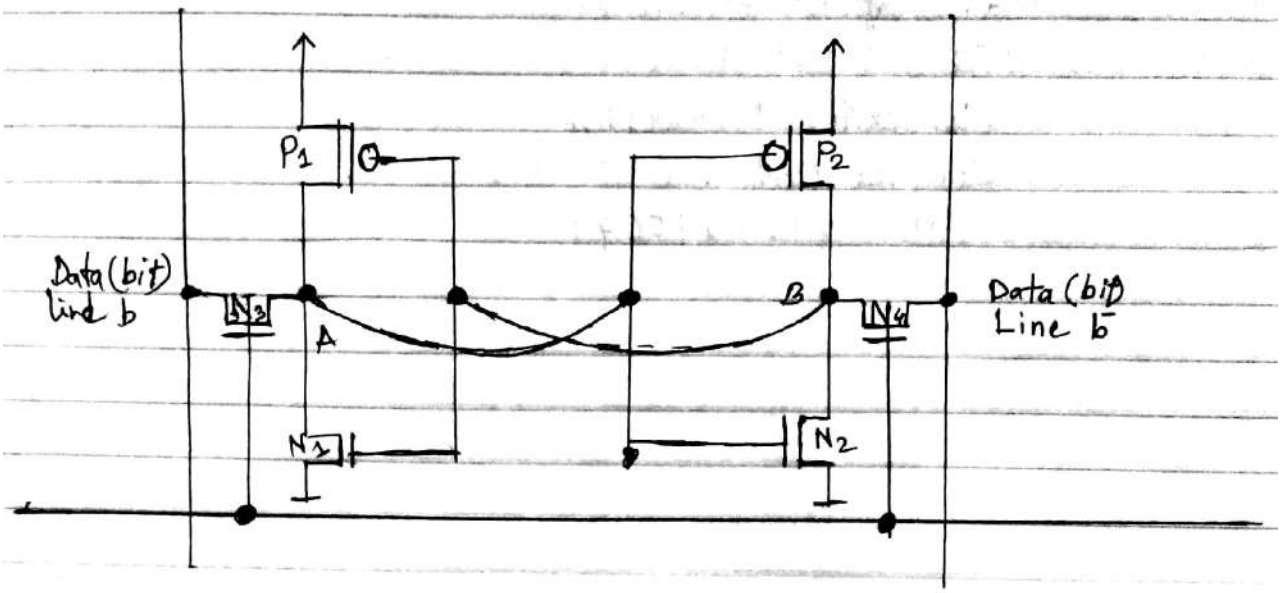
② A read signal is issued by the cpu.

③ The required word will be loaded by the memory into the MDR ready for use by the CPU.

(b)

Ans. to the Q no - 2(b)

* Cache read operation:—



① Both lines 'b' and 'b̄' are precharged high.

② The word select line is activated, thus turning on both transistors N_3 and N_4.

③ Depending on the internal value stored in the cell, point A (B) will lead to the discharge of line b (b̄).