Victoria University of Bangladesh

Department of computer Science & Engineering

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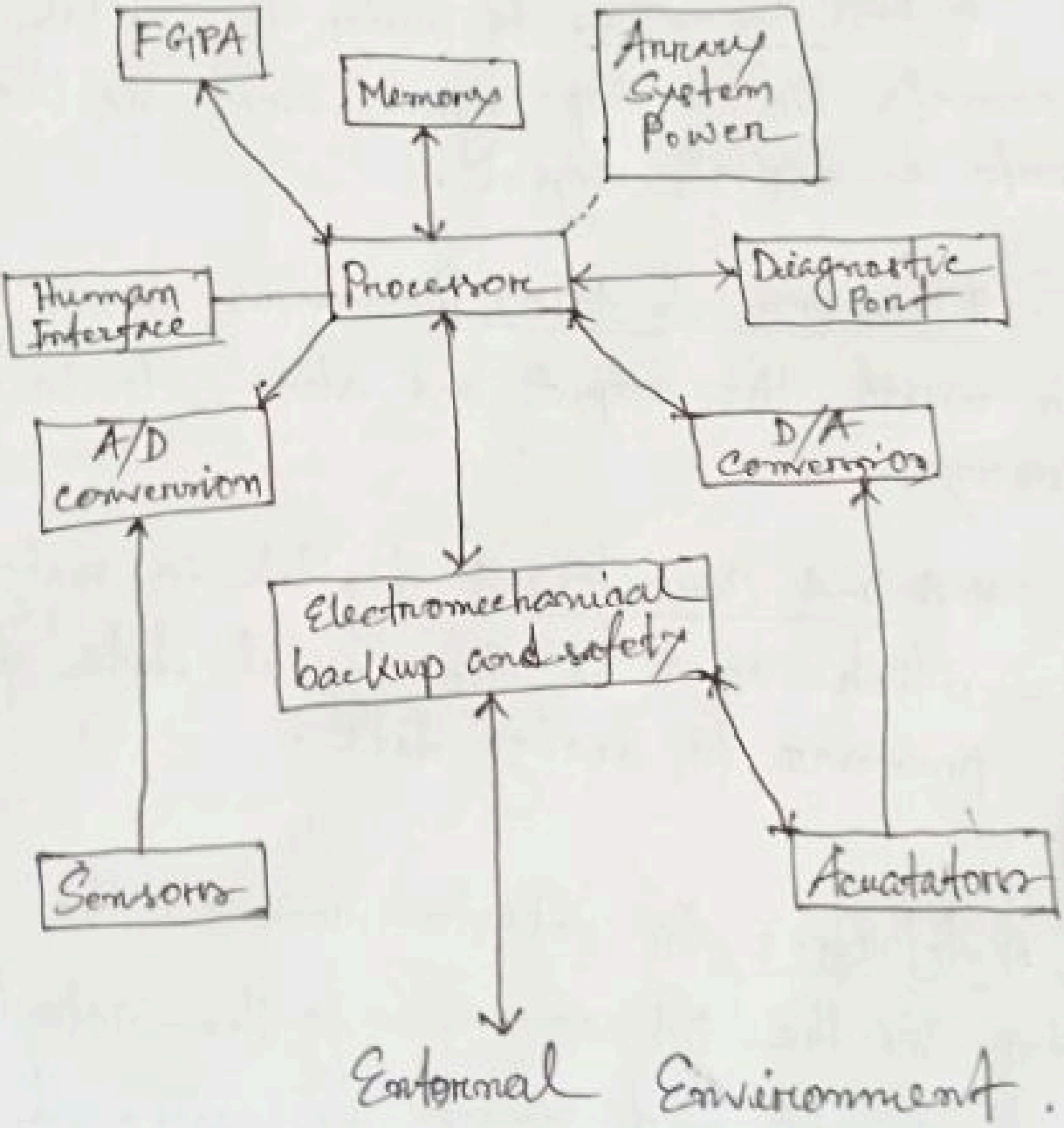
Course Title: Computer Architecture.

Mid-term Assessment

Answer to the question no: (1) (a)

# Here is a diagram of Possible Organigation of an Embedded System:-



* Sensors:- It measures the physically quantity and converts it to an electrical signal which can be read by an observer, or by an A2D converter.

# A-D Converter: An analog to digital converter converts the analog signal sent by the sensor into a digital signal.

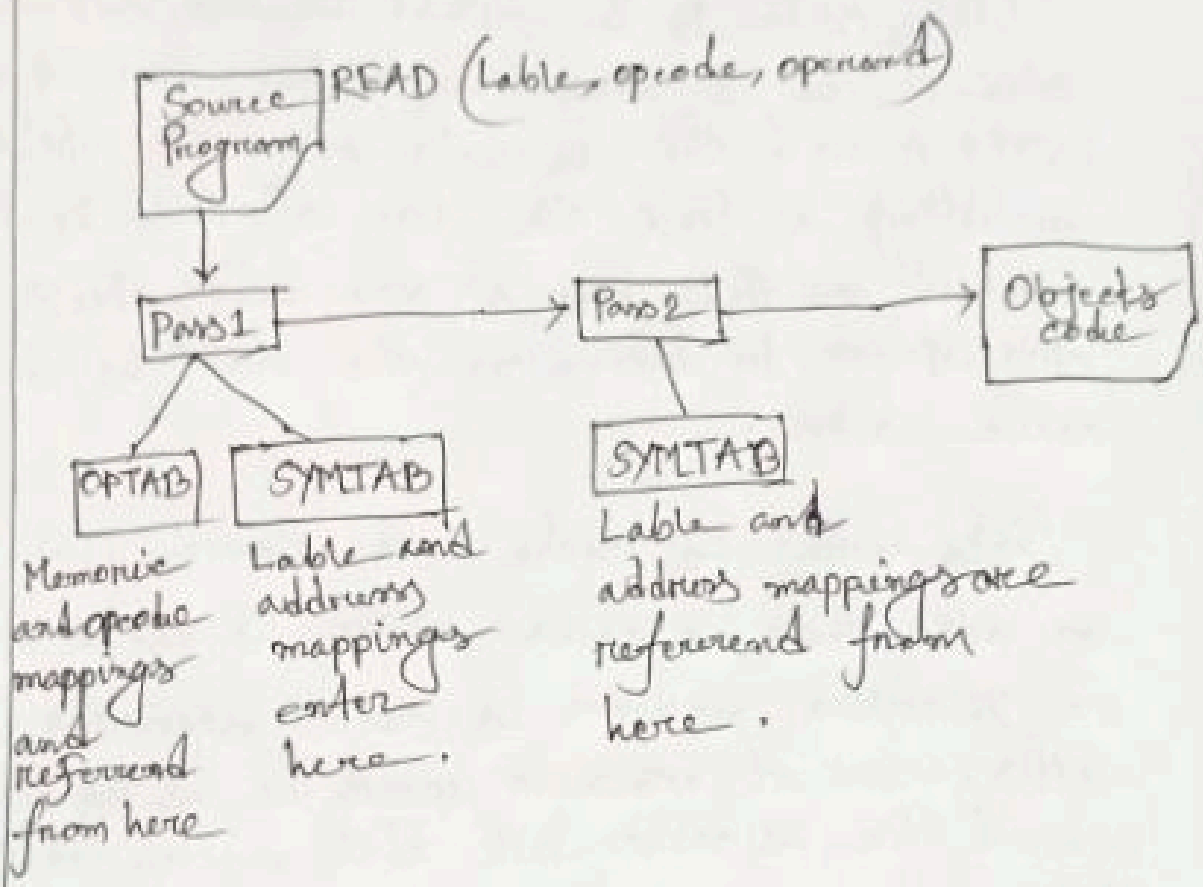
# Processor & ASICs: Processors process the data to measure the output and store it to the memory.

# D-A Converter: A digital to analog converter which converts the digital data fed by the processor to analog data.

# Actuator: An actuator compares the output given by the DA converter to the actual output stored in it and stored the approved output

Answer to the question no: 2 (b)

* A simple two pass assembler implementation:-




A two pass assembler solves this dilemma by devoting one pass two to exclusively resolve all (data/lable) forward references and the generat objects code with no hassles in the next pass. If a data symbol depends on another depends on yet another, the assembler resolved this recursively.

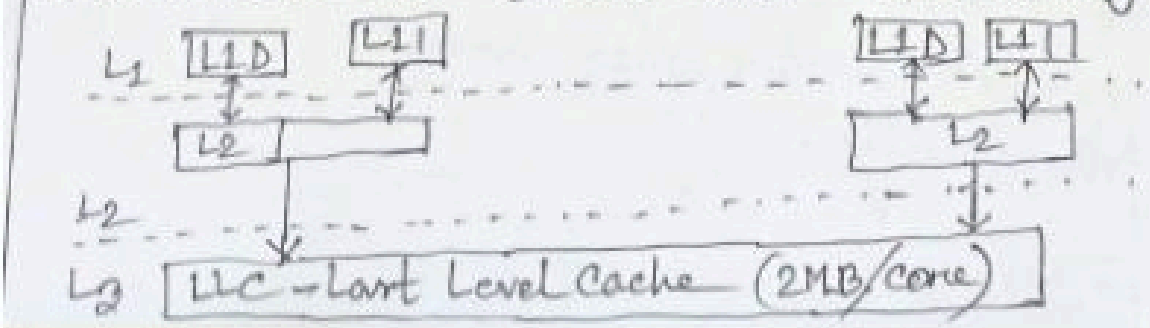
Answer to the question no: 1 (c)

* Three - level cache organization:—

(1) $L_1$ cache: It the fastest memory that is present in a computer system. CPU is most likely to need the $L_1$ cache at first while completing a task. The size of the $L_1$ cache depends on the CPU so you must check the CPU specs to determine the exact $L_1$ memory cache size.

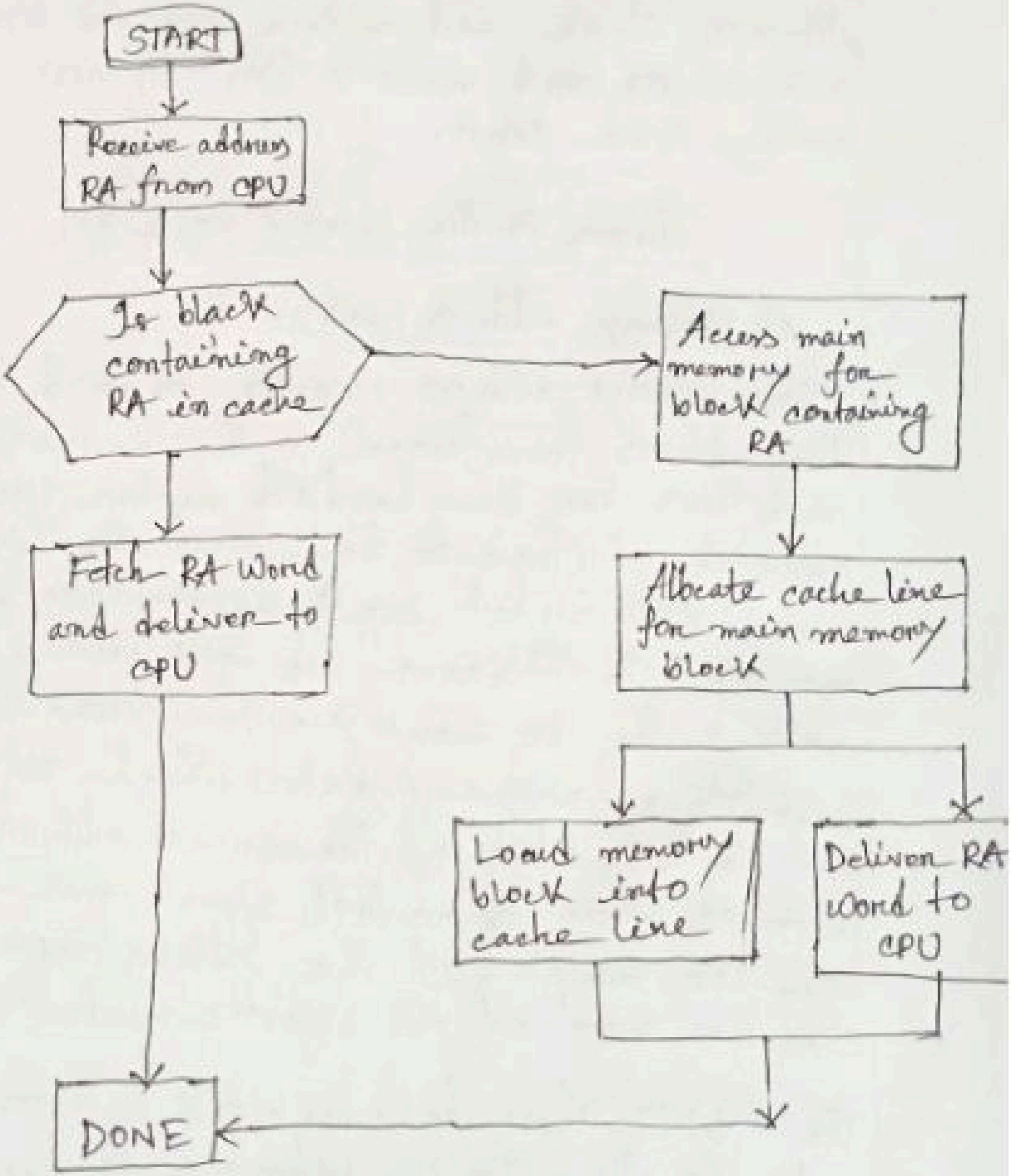
(2) $L_2$ cache: $L_2$ cache is slower and bigger in size than $L_1$ cache. Where $L_1$ cache measures in kilobytes, modern $L_2$ caches measures in mega-bytes. When it comes to speed the $L_2$ caches lags behind the $L_1$ cache but still much faster than RAM.

(3) $L_3$ cache: In the early days the $L_3$ memory cache was actually found on the mother board. Now, the $L_3$ cache can be massive, with top-end consumer CPUs featuring $L_3$ cache up to 32mb. The $L_3$ cache is the longest and slowest. Modern CPUs include the $L_3$ cache on the CPU itself.



Answer to the question no: 2 (b)

# Cache Read Operation :-



START Receive address RA from CPU is block containing RA in cache? No access main memory for block containing RA Yes fetch RA word Allocate cache and deliver line for main deliver RA word memory block to CPU into cache line DONE.

Answer to the question no: 2 (a)

# Memory address register:

The memory address register is used to handle the address transferred to the memory unit, and this can be handled either using a bus approach (which we have used in this architecture) or direct input declaration for the memory. In this case we will use a bus setting for the memory, therefore, the MAR becomes a simple register which sets its output to the value of the required address from the IR or PC when its control signal mar_load is high. For Example, if the address requires 8 bits than the size of the register needs to be 8 bits wide.

The "MAR" therefore, has clock and reset signals, and also the same interface to the internal processor bus (mar_bus) defined as a standard [illegible] however only the first