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ID: 2121210041
CSI:-427 (VLSI design and Analisis

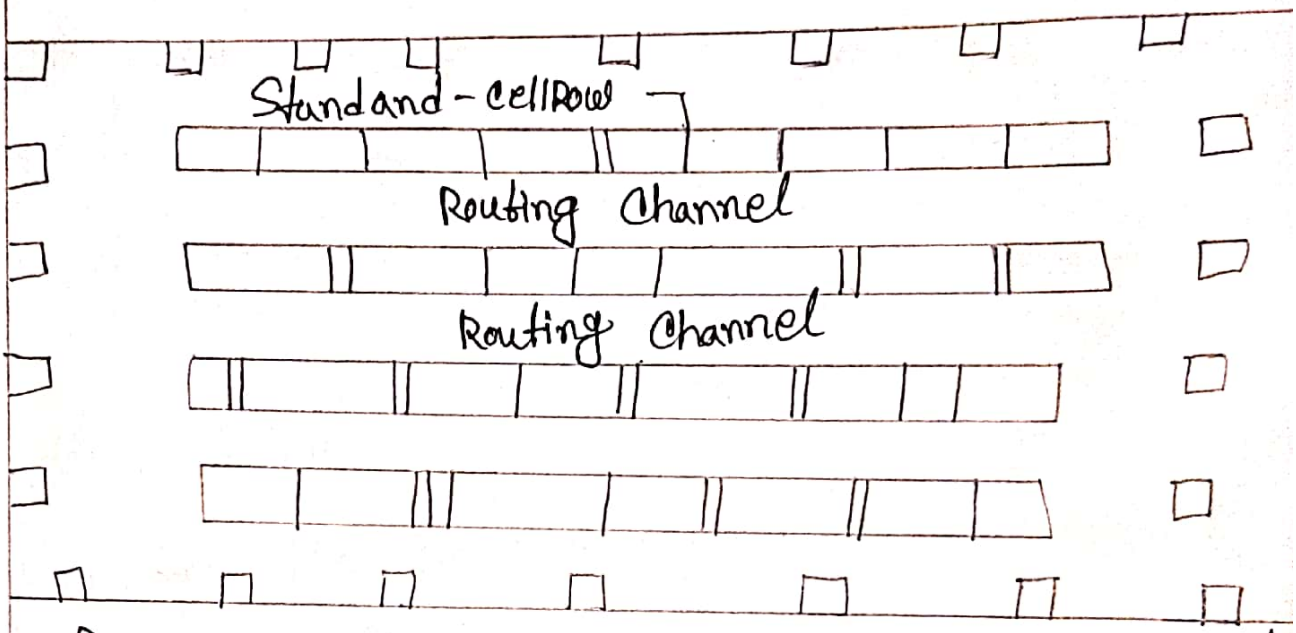
1. A

Ans

Standard Call Based Deeign:- A Standard Cell befed design requirs developent of to foll Custom mark yet. the Standerd Call is also Know as the Polycell. In this opprach all of the Commonly used lagie cella and. dereloped Charecteind and Stored in a Standrd cell ilibrary.

Alibary may Contain ofew hundred cell including inverters, NAND, NOR compley AOI, OAI Yates D- latches and Flip-flops Each gate type Each gate Can be implemented in Severel versions to provide adepush driving Capability for different to from the inventes gate can have Standard Size doulde and quadruple Size So that the chup denigner Can Select the Poper Size to obtain nigh Circuit Speed and layout.

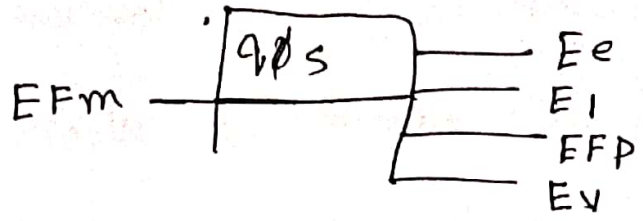
density Each All the aceroding to Several diffrent catogories such as.



figuis:- Fluor Plan Standand Cell besed desigh

(i) Delay time versus loud capacitance.
(ii) circuit simulation model.
(iii) Timing Simulation model.
(iv) fault Simulation model.
(v) Cell data for Plces-and route.
(vi) mas R data.
(vii) Automated Placement of the cell. and routing.

P.-04 A voltage called electromtives foree is quantitive expression of the potential. differeneres chanye between two Points



Øs = Safnes

Consider the Cross Sectional view of chaneel

Vs=VB=0 to Epm = Qms — EFP

Vc=(y=0)=Vs (oandVc (y=2)

the spatial yepmetry equation made

in dicate

$$dn = \frac{dy}{Q\,msy} \times 10^{-7}\ cm$$

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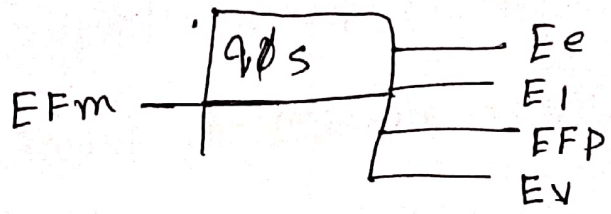

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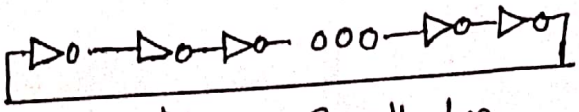
2-0A

Oscilation Solution:-



Ring oscillator

The logical effort of the inverter is g=1 by defination. the electric effort of each inverter is also 1 because it drive single identical load. the Prasitic delay is also 1.

The delay of each Statoge is

$$d = gh + p$$
$$= 1 \times 1 + 1$$
$$= 2$$

An N-stage ring oscillator has a period of 2N stage delays because a value must propagate twice around the ring ring to regain the orginal Polarito.

P.T.O

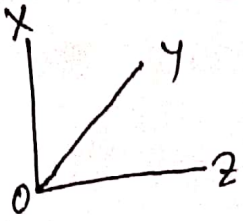
Therefore the period is $T = 2 \times 2N$ The freupesy is the of the period $1/4n$

A31-Stge ring oseillator in a 65nm Proees has a frequeney $1/(4 \times 31 \times 3) = 2.7$ GHz

note that ring oseilltors are often used as process monitors to Tedge if a Pontiaud Chip is fastor or Slower the nominally ex Deeted one the Inventrs Shoud be Replead with the nomim neplead with NAND gate to turn the ring.

2.B

Ans: Linemn-delay model Invi 2:-



This post teks about logical effort and Parasitte delay in linear delay model in VLSI. as was show befor dally linealy depend on the sum of the gate. normaliz-ed delay expresed as the sum of Parasitic delay p and effort delay fd = p+f the effor dalay depends on the fan-out not the gate f = gh here g is a logical. effort whatis fan-out or electrical effort was driving anale nidetical way.

⊕ In general the propagation delay of a gate can be written as $= f + p$

p is the delay due to intrinsic capacitance

f is the effort delay or stage effort and depends on the complexity and fanout of the gate.

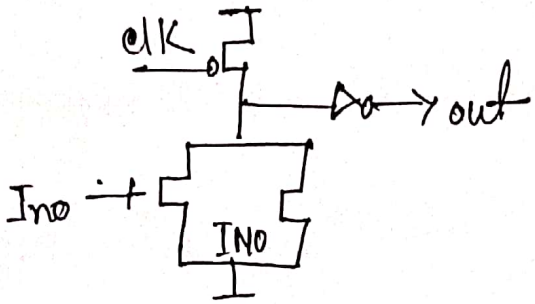
⊕ The stage effort is $f = gh$ with the complexity represented by the logical g.

⊕ An inverter is defined to the have logical effort of 1.

⊕ A gate driving n identical copies of itself is said to have an electrical effort h.

⊕ The electrical effort of non-identical copies of the gate or any type load to be $h = C_{out} / C_{in}$.

3.A Domino nose doudgets:- The nepid aduntang in VLS Mcont in Domina with block Dinganve



Domina Cute.

Daning the preehanye phase when the clock is low the pre Changing gots ON and the dynomie node is Commected to the VDD and gets prehonge to VDD whan olck yoes high the evelation Phae stor and the out Put yets evalted with the Pall down network and Condfionly the above Proposed Circut nas redaie no.

The Domino logic Stage Consists of Loge relalized using N-mos pull down network pull up the work Consists of a single pre Chanege dynamie node to logic high as shown - the dynamic nood is Casecad into stated noise Inverto and Con be connected. The Compen Stan Called kooper is used. In the first Domino Prosal the gate of the keeper is Connected to the ground.

4.A Souree of power Dissipation: The power dissipation in cmos Circnts Comes form two Components.

① Dynamic disbipation.

② Static dissi pation.

Dynamic:- ① due to choging an dis choging load Capacitance as yats switch.

② short circuit while to the from of Lekaye eamrent when the System is ont powend on is in stan by o mod in circuts there are seveal Sourc of lekoge Sumrent including subthe subtheaded Leakage. dide lekoges around tromsis and n-wells tamel Cannent ghte lekge cto. Pdnome in Aefive. effot the dynamic Powen.

Static Power :- When a cmos circuit is in an Idle State there is Still Some Stated Power dissipation. In a silicon Chip ther are millions of trns / tors and the Cournent is Compible to lekage and Sub-threshold Cornents depend upon Processing Dramefors.

$I_{revens} = A.J_s (eK^{I}_{1})$

A is the tuntins area.

Q is the Chargs of electoon

K is openting tem patune.

Diode formation due to mos Structe Structure is in herent in. cease in temDenatue millions of tansiton to the stafic. Power dissipation.