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Batch : 17th
Course Code : CSE-427
Course name: VLSI Design

VLSI Design : CSE-427

(2) Ans to the Que No: 01

Ans: Floor Planning

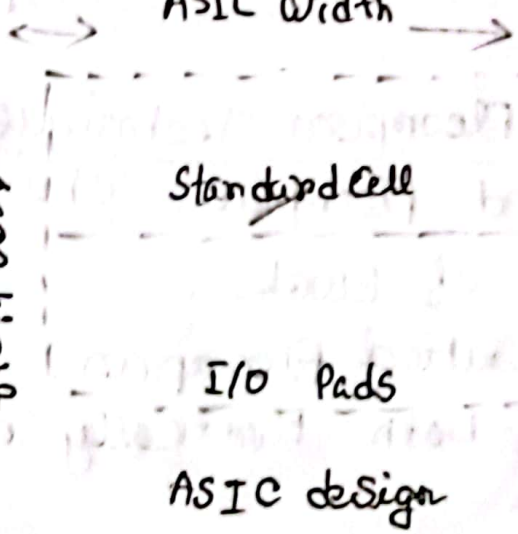
floorplanning is the art of any physical design. A well and perfect floorplan leads to an ASIC design with higher performance and optimum area.

floorplanning can be challenging in that, it deals with the placement of I/O pads and macros also well as power and ground structure.

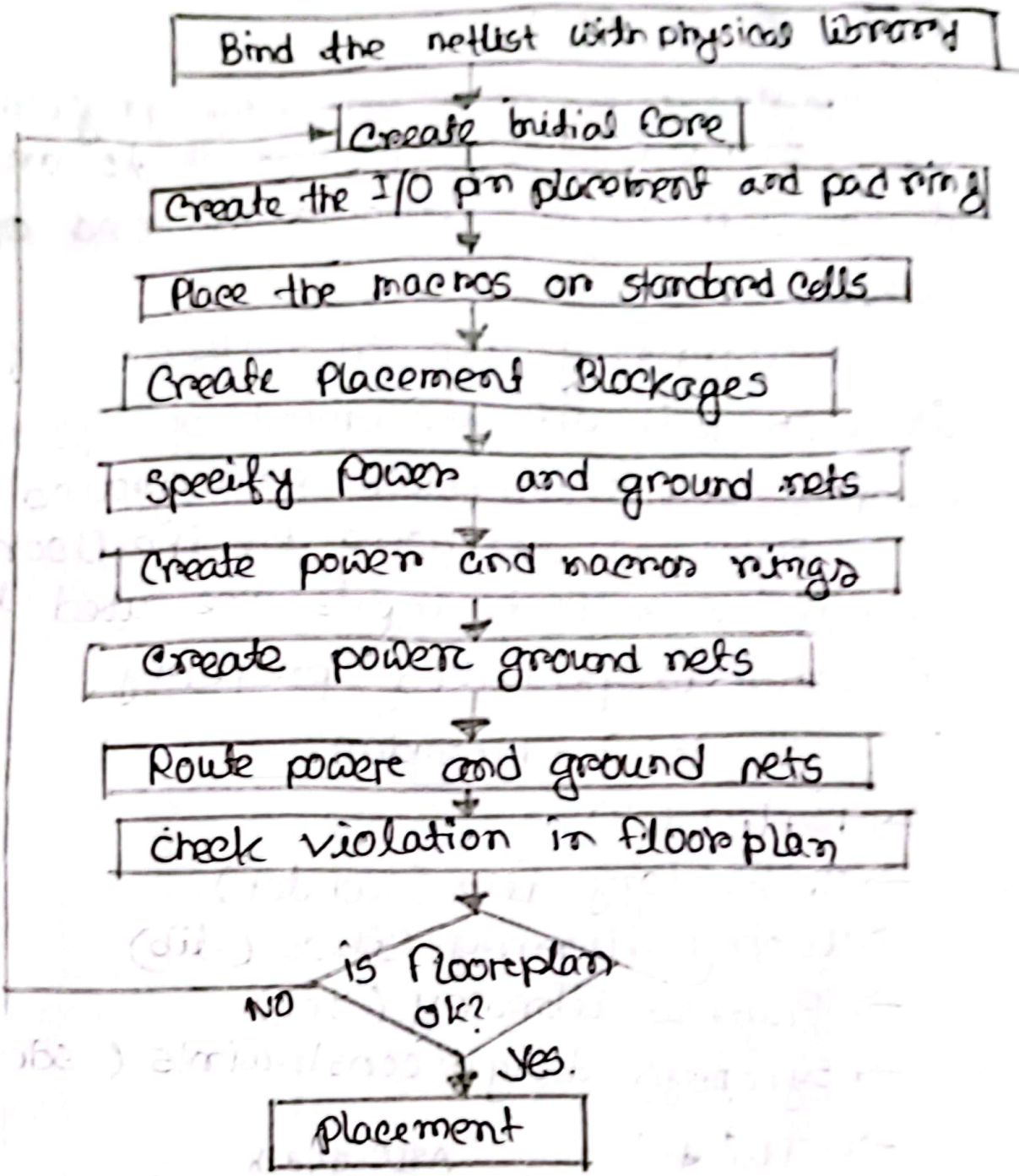
Before we are going for the floor planning to make sure that inputs are used for floorplan is prepared properly.

Inputs for floorplan:

→ Netlist (.v)
→ Technology file (techdef)
→ Timing library files (.lib)
→ Physical library (.lef)
→ Synopsys design constraints (.sdc)
→ TLU+



ASIC design



Types of Floorplan Techniques:

→ Abutted floorplan : channel less placement of Blocks.

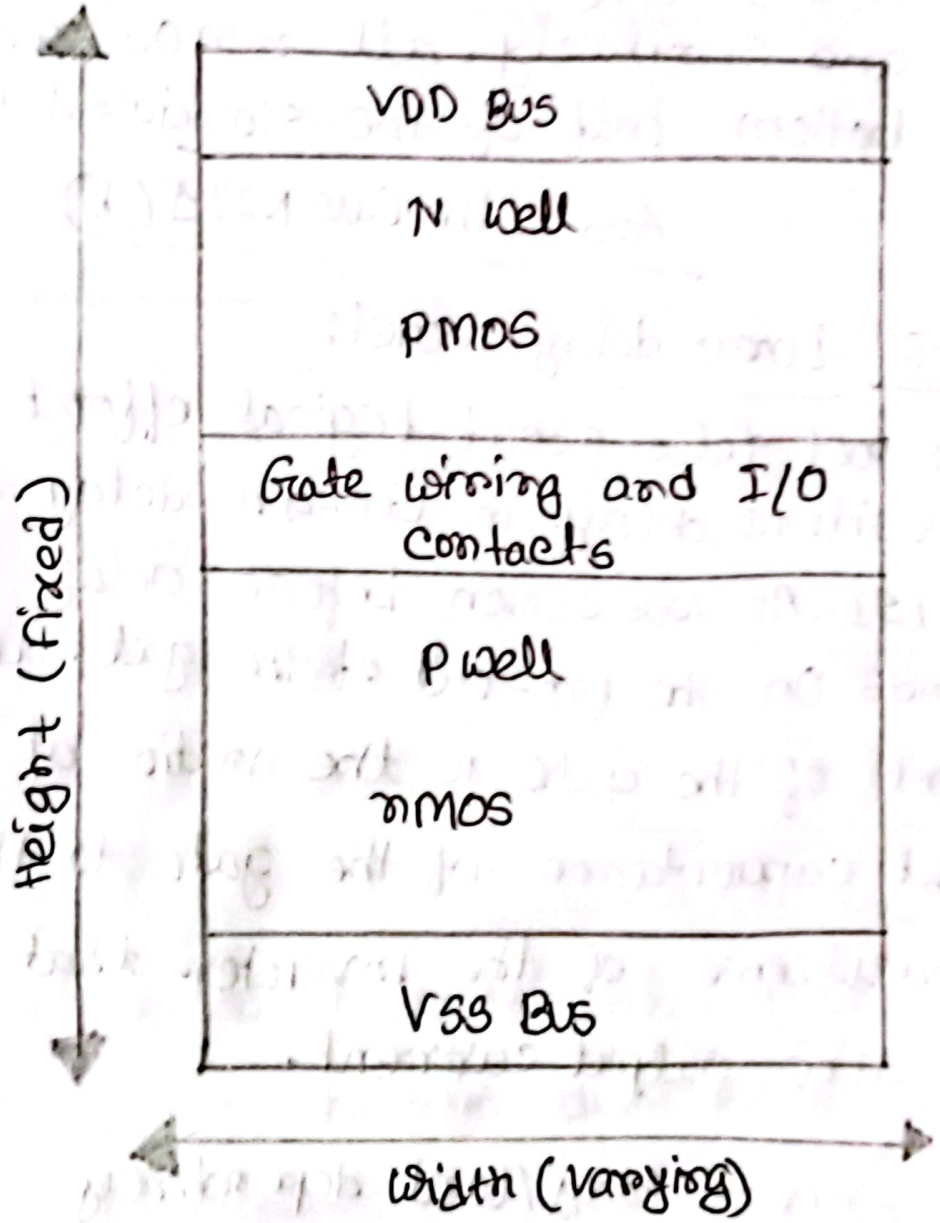
→ Non-abutted floorplan :

→ Mix of both : Partically abutted with some channels

(3)

Standard cells in ASIC Design :

Standard cells are well defined and pre-characterized cells used in ASIC (Application Specific Integrated Circuit) Design flow as basic building blocks. All these cell are equal in height and can easily fit into the standard cell row. Standard cells are highly reusable and save lots of ASIC design time.



Ans to the Qus NO: 01 (b)

Answer: Two different equations for the current through voltage-dependent capacitances are used in the literature. One equation is obtained from the time derivative of charge that is considered as capacitance-voltage product:

$$dQ/dt = d[C(V)V]/dt\,[dV/dt] + V[dC(V)/dt].$$

In the second equation, the term $V[dC(V)/dt]$ does not exist: $dQ/dt = C(V)[dV/dt]$. This paper clears the ongoing confusion caused by the difference between these two equations. We use the voltage-dependent parasitic capacitance of a commercial Schottky diode in reverse bias mode to test experimentally both equations. The result is that it is incorrect to add the term $V[dC(V)/dt]$ in the first equation with the measured capacitance. We also perform a theoretical analysis, which shows that the differential capacitance, $C(V) = dQ/dV$, in the correct current equation corresponds to the physical parameters of the diode capacitance.

Ans to the Qus NO: 2 (a)

2(a): An oscillator is used to generate a signal which has a specific frequency, and these are useful for synchronizing the computation process in digital systems. It is an electronic circuit that produces continuous waveforms without any input signal. The oscillator converts a DC signal into an alternating signal form at the desired frequency. The definition of the ring oscillator is "an

odd number of inverters are connected in a series form which with positive feedback & output oscillates between two voltages levels either 1 or zero to measure the speed of the process. In place of inverter we can define it with NOT gates also. These oscillators have an 'n' odd number of inverters. For instance, if this oscillator has 3 inverters then it is called a three-stage ring oscillator. If the inverter count is seven then it is seven stage ring oscillator. The number of inverter stages in this oscillator mainly depends on the frequency which we want to generate from this oscillator.

"Ring-oscillator uses an odd number of inverters to acheive more gain than a signal single inverting amplifier. The inverter gives a delay to the input signal and if the numbers of inverters are increased then oscillator frequency will be decreased. So the desired oscillator frequency depends on the number of inverter stages of the oscillation."

This frequency of oscillation formula for this oscillator is $f = \frac{1}{2nT}$

Here, T = Time delay for signal inverter
n = number of inverters in the oscillator.

Ans to the QUS NO: 02 (b)

(b) Linear delay model:

→ Linear delay / load dependency.
→ Relatively accurate i.t.
→ Widely used for timing driven tools flows
→ Linear slew effects are commonly added to improve the model

→ In general the propagation delay of a gate can be written as: $d = f + p$
- p is the delay due to intrinsic capacitance.
→ f is the effort delay or stage effort and depends on the complexity and fanout of the gate.

The stage effort is: $f = gh$ with the complexity represented by the logical effort g.
→ An inverter is defined to have a logical effort of 1.
→ More complex gates have greater logical effort indicating that they take longer to drive a given fanout.

Ans to the Qus No: 03 (a)

Domino noise budgets:

Domino logic is attractive for high-speed circuits

→ 1.5 – 2× faster than static CMOS

→ But many challanges

- Monotonicity
- Leakage
- Charge sharing
- Noise

→ Widely used in high performance microprocessors.

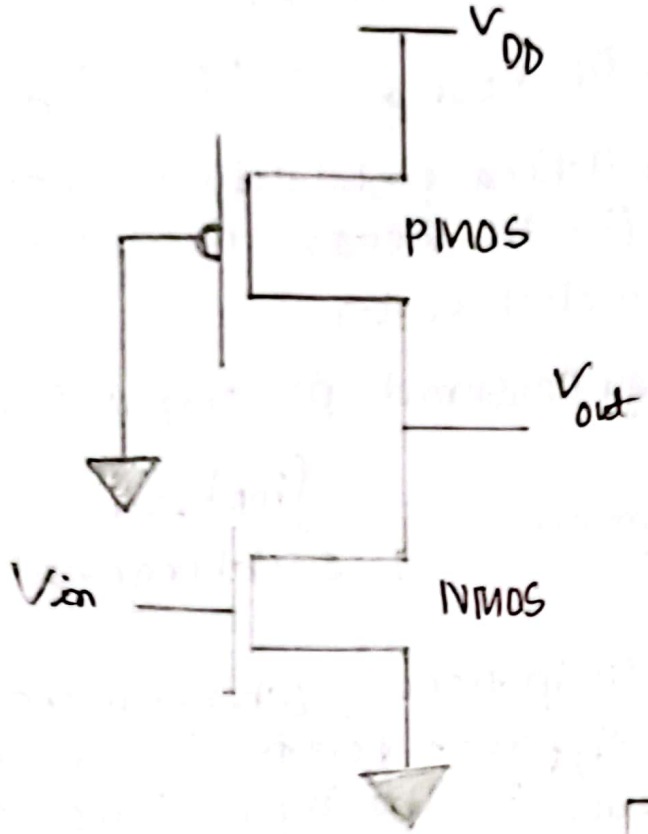
Domino Noise budgets:

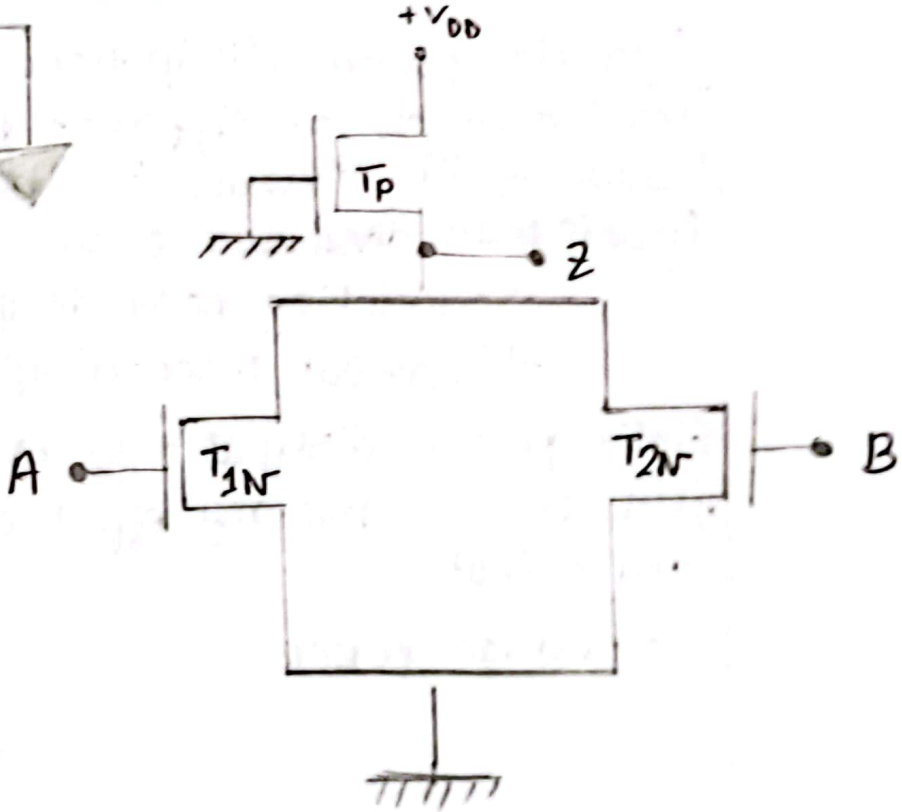
- Charge leakage
- Charge sharing
- Capacitive coupling
- Back-gate Coupling.
- Minority Carriers injection
- Power Supply Noise
- Soft errors
- Noise feedthrough
- Process corner effects.

Ans to the Qus No: 03 (b)

Answer:

Pseudo NMOS inverter:





NMOS NOR →

Ans to the QUS NO: 01 (a)

The power dissipation in a CMOS logic gate can be expressed as

$$P = P_{state} + P_{dynamic}$$

$$= (V_{DD} \cdot L_{leakage}) + (P \cdot f \cdot E_{dynamic})$$

Where p is the switching probability or activity factor. at the output node (i.e. the average number of output switching events per clock cycle)

The dynamic energy consumed per output switching event is defined as

$$E_{dynamic} = \frac{\int i_{DD} V_{DD} dt}{I - switching\ event}$$

Dynamic power dissipations: Whenever the logic level changes at different points in the circuit because of the changes in the input signal at the dynamic power dissipation occurs.

- → Switching power dissipation
- → Short cut power dissipation

Static power dissipations: This is a type of dissipation which does not have any effect of level change in the input and output

- → Leakage power.