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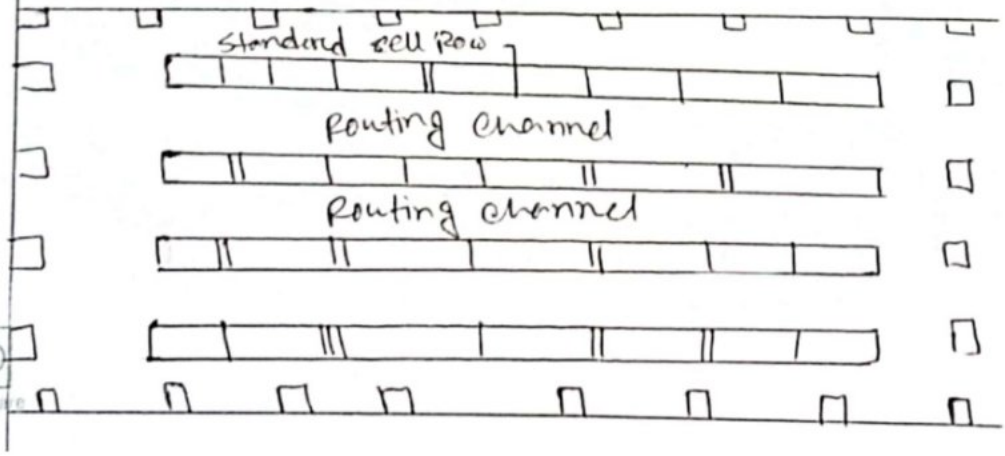
CSI : 427 (VLSI design and Analysis)

Ans to the Qus no 1 (a)

Standard call based design: A standard call based design requires developent of to full custom mark yet. The standard call is also know as the polycell. In this approch all of the commonly used logic cells and developed characteind and stored is a standard cell library.

A library may contain a few hundred cell including inverters, NAND NOR Compley AOI, OAI yates D-latches and flip-flops Each gate type. Each gate can be implemented in several versions to provide adepush driving capability for different to from the inverters gate can have standard size double and quadruple size. so that the chip designer can select the popere size to obtain high circuit speed and layout. Density each all the according to several diffrent catalogies such as.



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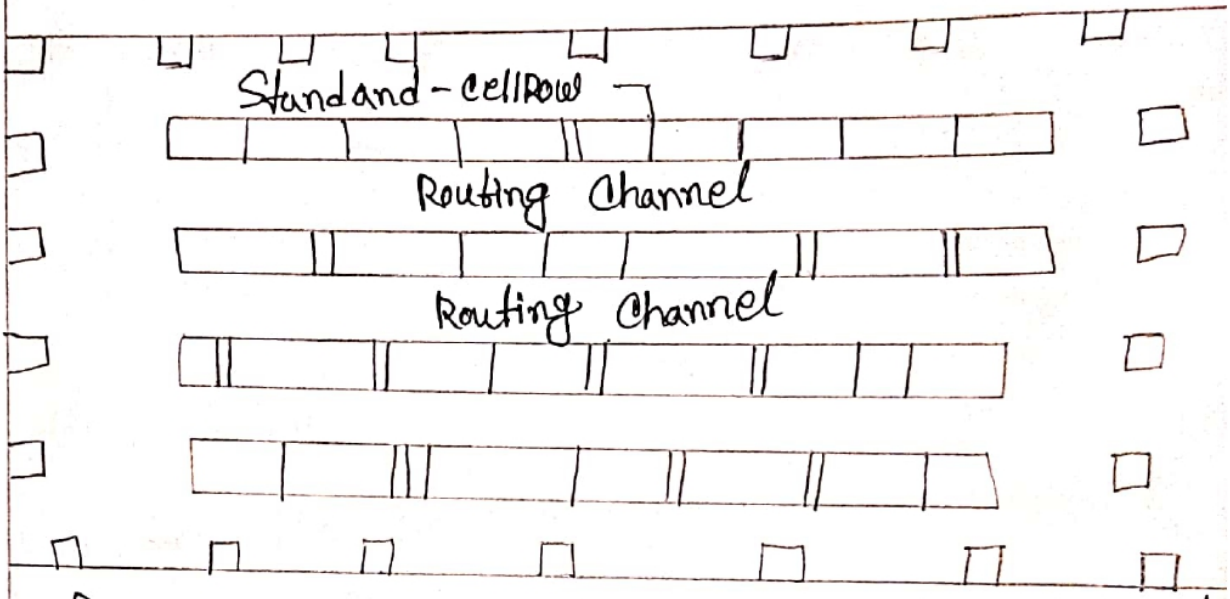
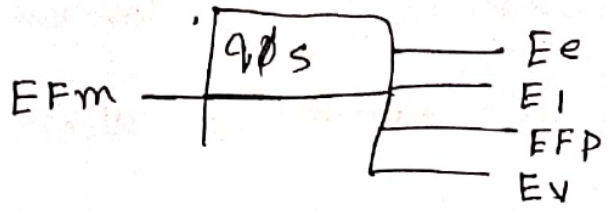


figuis:- Fluor Plan Standand Cell besed desigh

(i) Delay time versus loud capacitance.
(ii) circuit simulation model.
(iii) Timing Simulation model.
(iv) fault Simulation model.
(v) Cell data for Plces - and route.
(vi) mas R data.
(vii) Automated Placement of the cell. and routing.

P.-04 A voltage called electromotives force is quantitive expression of the potential. differences change between two points



Øs = Safres

Consider the cross sectional view of channel

Vs = VB = 0 to Epm = Qms − EFP

Vc = (y = 0) = Vs (and Vc (y = 2)

the spatial yepmetry equation made

in dicate

$$dn = \frac{dy}{Ø_{msy}} \times 10^{-7} \text{ cm}$$

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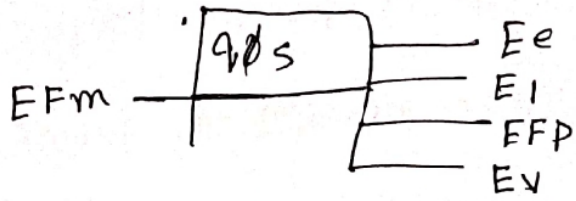

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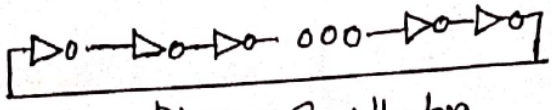
2-04

Oscilation Solution:-



Ring oscillator

The logical effort of the inverter is g=1 by defination. the electric effort of each inverter is also 1 because it drive single identical load. the Prasitic delay is also 1.

the delay of each stage is

$$d = gh + p$$
$$= 1 \times 1 + 1$$
$$= 2$$

An N-stage ring oscillator has a period of 2N stage delays because a value must propagate twice around the ring ring to regain the orginal polarito.

P.T.O

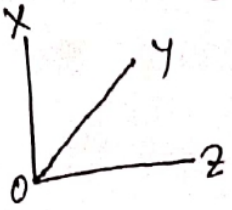
Therefore the period is $T = 2 \times 2N$ The freupesy is the of the period $1/4n$

A31-stage ring oseillator in a 65nm Proees has a frequeney $1/(4 \times 31 \times 3) = 2.7$ GHz

note that ring oseillators are often used as process monitors to Tedge if a Pontiac chip is fastor or Slower the nominally ex Deeted one the Inventrs Shoud be replead with the nomim replead with NAND gate to turn the ring.

2.B

Ans: Linemn-delay model Invi 2:-



This post teks about logical effort and Parasitte delay in linen delay model in VLsi. as was show befor dely linealy depend on the sum of the gate. normaliz-ed delay expresed as the sum of Parasitc delay p and effort delay fd = p+f the effor dalay depends on the fan-out not the gate f = gh nere g is a logical. effort whatis fan-out or electrical effort was driving anale n idetical way.

(#) In general the propagation delay of a gate can be written as $= f + p$

p is the delay due to intrinsic capacitance

f is the effort delay or stage effort and depends on the complexity and fanout of the gate.

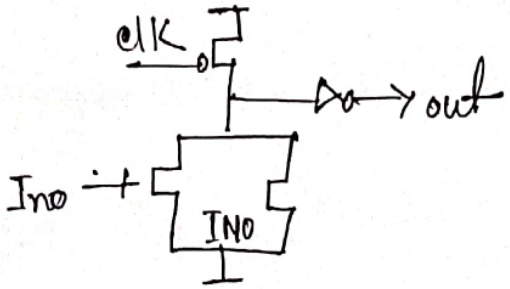
(#) The stage effort is $f = gh$ with the complexity represented by the logical g.

(#) An inverter is defined to the have logical effort of 1.

(#) A gate driving n identical copies of itself is said to have an electrical efforth.

(#) The electrical effort of non-identical copies of the gate or any type load to be $h = C_{out} / C_{in}$.

3.A Domino rose doudgets:- The nepid aduntang in VLS Mcont in Domina with block Dinganve



Domina Cute.

Daning the preehange phase when the clock is low the pre Changing gots ON and the dynomie node is Commected to the VDD and gets prehonge to VDD whan olock yoes high the evelation Phae stor and the out Put yets evalted with the Dall down network and Condtionly the above Pro Posed Circut nas redaie no.

The Domino Logic Stage Consists of Logic relatized using N-mos pull down network pull up the work Consists of a single pmos Chanege dynamic node to logic high as shown - the dynamic node is Cascad into stated noise Inverto and Can be connected. The Compensation Called kooper is used. In the first Domino Prosal the gate of the keeper is Connected to the ground.

4.A Source of Power Dissipation: The Power dissipation in Cmos Circuits Comes from two Components.

(i) Dynamic disbipation.

(ii) Static dissi pation.

Dynamic:- (i) due to choging an dis choging load Capacitance as yats switch.

(ii) Short circuit while to the from of Lekage current when the System is ont Powerd on is in stan by o mod in Circuits there are several Sourc of lekoge Current including subthed Subtheaded Leakage. dide lekoges around thomsis and n-wells tamel Current ghte lekge eto. Pdnome in Refive. effot the dynamic Power.

Static Power:- When a cmos circuit is in an Idle State there is Still Some Stated Power dissipation. In a silicon Chip then are millions of trns/tors and the Cournent is Comprble to lekage and Sub-threshold Cornents depend upon Processing Dramefors.

$P_{evens} = A.J_s (e^{K/T_1})$

A is the tuntins area.

Φ is the Changs of electoon

K is operting tem patune.

Diode formation due to mos ~~Struck~~ Structure is in herent in. cease in temDenatue millions of tunsiton to the stafic. Power dissipation.