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CSE-427- VLSI Design
Final Examination - Summer-2022

Q-01

1.A

* Ans to the Qs no: 1.A *

Standard Cell Based Design:- A standard cell based design requires development of a full Custom Mask yet. the standard cell is also know as the polycell. In this approach, all of the commonly used logic cells are developed, characterized and stored in a standard cell library.

A library may Contain a few hundred cell including inverters, NAND, NOR complex AOI, OAI gates. D-latches and Flip-flops. Each gate type can be implemented in several versions to provide adequate driving capability for different fan-outs. The inverters gate can have standard size, double and quadruple size so that the chip designer can select the proper size to obtain high circuit speed and layout density Each All the acerodin g to several different categories such as.

P.T.O

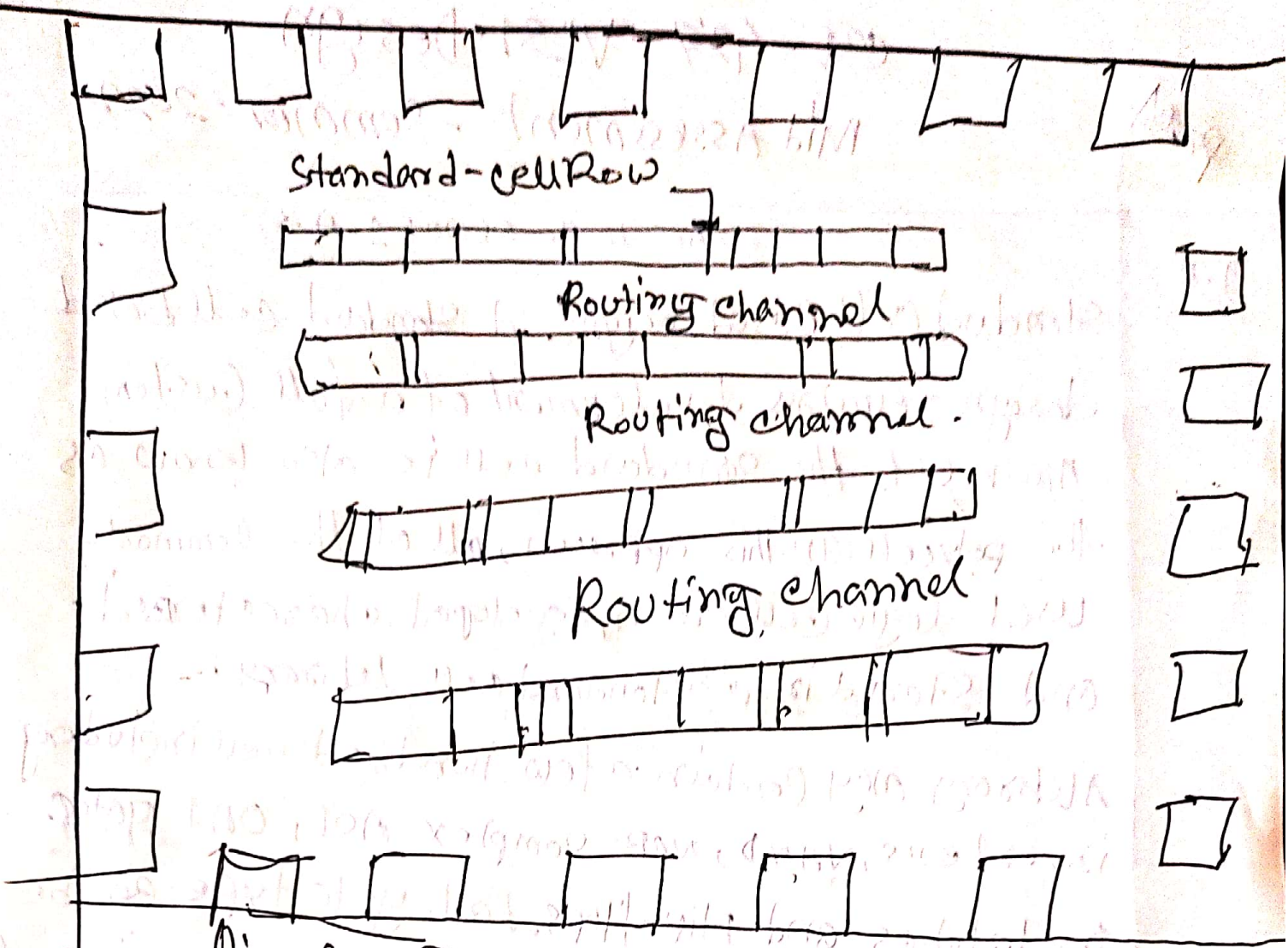


figure:- Floor plan standard cell based design

(I) Delay time versus load capacitance
(II) Circuit simulation model
(III) timing simulation model
(IV) fault simulation model
(V) cell data for place-and-route.
(VI) Mask data
(VII) Automated placement of the cell and routing.

1.B

P-03

Ans to the QS no: 1.B

Ans:- Equation of voltage dependence or Equation applied in this based on the project.

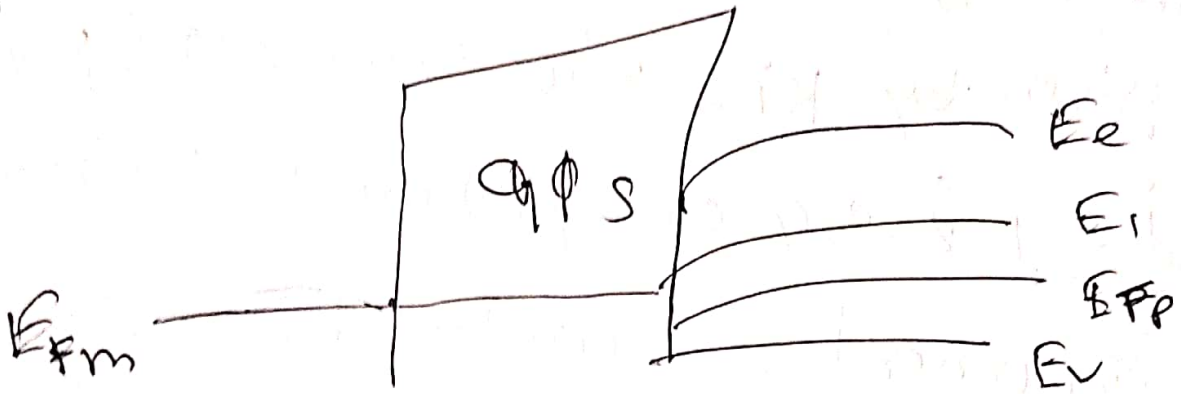
the voltage of the equilibrium constant is given by $K_i = K_{iO} \exp(ZiFV\beta)$ $(i = 1, 2, 3, 4, \text{or } 5)$ where K_{iO} is the component and constant K_i and Z_j is its voltage dependence. Each of curves is a mean obtained from five oocytes. the curve was fitted to various equations as the between versus voltage.

$$\frac{1}{2} \cdot \sum_{i=1}^{n-1} (V_{i+1} + V_j)(\Phi_{i+1} - \Phi_j)$$

yields the total current density, in the leakage voltage.

P-04

A voltage called electromotives force is quantitiative expression of the potential difference charge between two points



Q_s = surface

consider the cross sectional view of n channel, $V_S = V_B = 0$ → $E_{Fm} = Q_{ms} - E_{Fp}$

$$V_c = (y=0) = V_S \text{ (and } V_c (y=L)$$

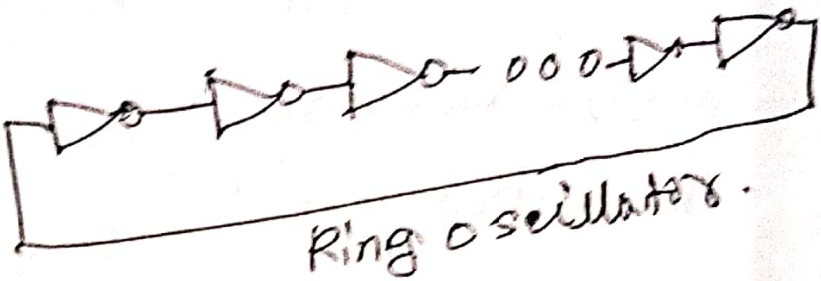
The Spatial geometry equation made indicate

$$dR = \frac{dy}{Q_{ms}} \times 10^{-4} \text{ cm}$$

P.05

Ans to the Qs no: 2 A

2.A Oscillator Solution:-



Ring oscillator.

The logical effort of the inverter is $g = 1$ by defination. The electrical effort of each inverter is also 1 because it drive a single identical load, The parasitic delay is also 1.

The delay of each stage is

$$d = gb + p$$
$$= 1 \times 1 + 1$$
$$= 2$$

An N-stage ring oscillator has a period of 2N stage delays because a value must propagate twice around the ring to regain the orginal polarity.

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Therefore the period is $T = 2 \times 2N$ The frequency is the of the period $1/4N$

A 31 - 'stage ring oscillator in a 65nm process has a frequency of $1/(4 \times 31 \times 3) = 2.7$ GHz

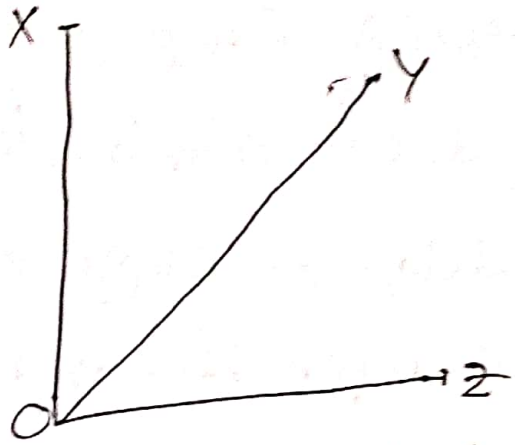
Note that ring oscillators are often used as process monitors to Judge if a particular chip is faster or slower than nominally expected, one of the inverters should be replaced with NAND gate to turn the ring.

** Ans to the Qs no: 2.B **

2.B

p-07

Ans: Linear delay model in VLSI:-



This post tells about logical effort and Parasitic delay in liner delay model in VLSI. as was shown befor daley linearly depend on the fan-out of the gate. normalized delay d of a gate can be expressed as the sum of parasitic delay p and effort delay fd = p + f The effort delay depends on the fan-out n of the gate f = gh here g is a logical effort. what is fan-out or electrical effort was driving a gate h identical way.

P-08

(#) In general the propagation delay of a gate can be written $d = f + p$

- p is the delay due to intrinsic capacitance

- f is the effort delay or stage effort and depends on the complexity and fanout of the gate.

(#) The stage effort is $f = gh$ with the complexity represented by the logical g.

(#) An inverter is defined to have a logical effort of 1.

(#) A gate driving h identical copies of itself is said to have an electrical effort h.

(#) The electrical effort of non-identical copies of the gate or any type load to be $h = C_{out} / C_{in}$

8.09

Logic effort :-

Type Gate	1 input	2 input	n input
Inverter	1		
NAND	0	$\frac{4}{3}$	$\frac{2+n}{3}$
NOR	0	$\frac{5}{3}$	$\frac{1+2n}{3}$
XOR	0	4	0
XNOR	0	4	0

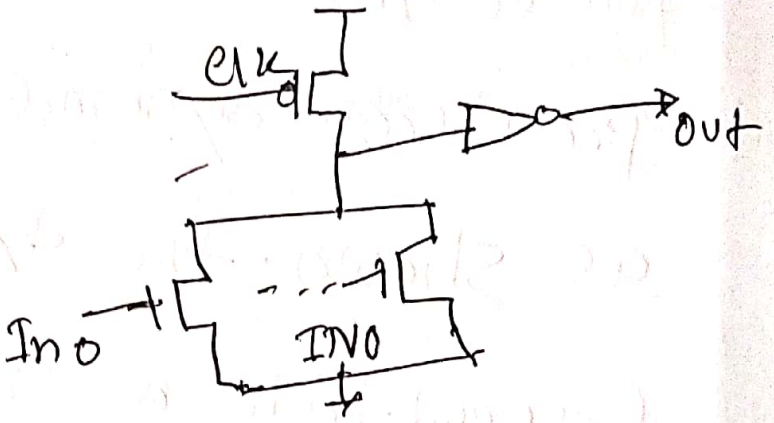
Parasitic delay of gates :-

Gate type	1	2	n
(I) Inverter	1	0	0
(II) NAND	0	2	n
(III) NOR	0	2	n

$$T = Re\left(\frac{n^2}{2} + \frac{5n}{2}\right)$$

Ans to the Qs no: 3. A

3.A **Domino noise budgets:-** The rapid advantange in VLSI Circuit in Domino with block Diagram.



∴ Domino Gate

During the precharge phase when the clock is Low, the pre charging gets ON and the dynamic node is Connected to the VDD and gets precharge to VDD. When clock goes high the evalation phase start and the output gets evaluted with the pull down network and Conditionally. The above proposed circuit has reduce no.

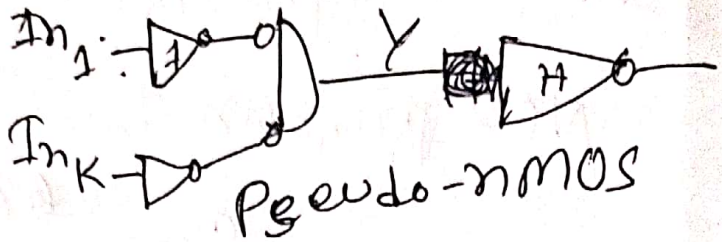
(P to)

The Domino Logic Stage Consists of logic realized using N-mos pull down network pull up the work Consists of a single pre charege dynamic node to logic high as shown. the dynamic node is Casecad into a static noise inverter. from where the gate output is taken and can be connected. The Compensate the leakage on node to weak transistor Called keeper is used. In the first Domino proposal the gate of the keeper is connected to the ground.

Ans to the Qs no: 3.B

3.B

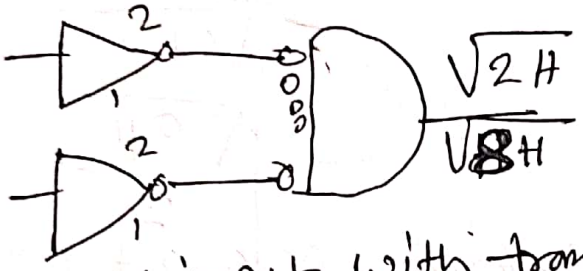
Solution Diagram:-



Pseudo-nMOS

K-input AND gate driving

Nmos Load H



K input with transistor.

Solution:- The path electrical effort is H and the branching effort is B = 1, The inverter has a logical effort of 1. the Pseudo-n-mos NOR has an average logical effort of 8/9. The path logical effort is $G = 1 \times (8/9)$

$a = 8/9$, so the path effort is $8H/9$. Each stage should bear an effort of $f = \sqrt{8H/9}$

Using the capacitance transformations gives NOR pulldown transistor widths of

$$C_{in} = \frac{C_{out}}{f} = \frac{(8/9)+1}{\sqrt{8H/9}} = \frac{\sqrt{8H}}{3}$$

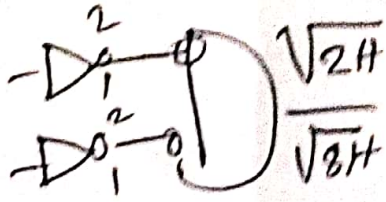


fig- 9.16 -

unit sized inverters. As a unit inverter has three units of input capacitance. the NOR transistor nMOS width should be $\sqrt{8H}$.

We estimate the average parasitic delay of a k-input pseudo-nMOS NOR to be $(8k+4)/9$

The total delay T is

~~$D = Nf + P$~~

$$D = nf + p = \frac{4\sqrt{2}}{3}\sqrt{H} + \frac{8k+13}{9}$$

Ans:-

4.A Source of power Dissipation:- The power dissipation in CMOS circuits comes from two components

(I) Dynamic dissipation

(II) Static dissipation

Dynamic:- (I) due to charging an discharging load Capacitance as gate switch.

(II) Short circuit current while both nmos and pmos.

the power dissipation occurs in the form of leakage current when the system is not powerd or is in standby mod. In circuits there are several sources of leakage current including Subthreaded leakage. diode lekages around transistor and n-wells tunnel current. gate leakage etc. $P_{dynamic} = P_{switching} + P_{circuit}$ power can be also consider in Active. Voltage has quadritic effort the dynamic power.

Static power :- When a CMOS circuit is in an idle state there is still some static power dissipation. In a silicon chip there are millions of transistors and the overall power dissipation due to leakage current is comprable to dynamic power dissipation. the valuese of lekage and sub-threshold currents depend upon processing parameters,

$$I_{reverse} = A \cdot J_s (e^{qkT} - 1)$$

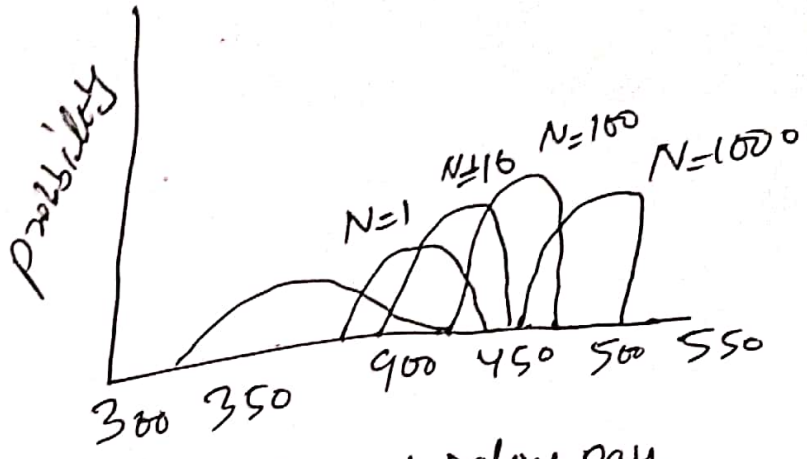
A is the juntions area.
q is the charge of electron
k is operating tempexature.

Diode formation due to mos structure is inherent, the result in leakage current this current increase in temperature. Millions of transistor to the static power dissipation.

Ans to the Q no: 4.B

4.B

Solution:-



Longest Delay Path

Table: 7.9:-

N	E(m)	Q(m)
2	0.56	0.82
10	1.54	0.59
100	2.50	0.43
1000	3.24	0.35
10,000	3.85	0.30
100,000	4.40	0.28

The Maximum of 100 standard normal random variables has an expected value of

value = 2.50
deviation = 0.43

Thuse the expected critical path delay with mean is $400 + 2.50 \times 20$
$= 450$ ps — (Ans)

and standard deviation $= 0.43 \times 20$
$= 9$ ps — (Ans) Ans: